Australian Black Box Electrical System for Recording and Later Recovery of Cockpit Voice and Flight Data in March 1962 Validation Flight Test

by

K.F. Fraser
Retired Principal Research Scientist
Defence Science and Technology Group Melbourne

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Summary

This document relates mainly to the electrical aspects of the Australian Flight Memory System (FMS) for which Dr David Warren is the recognized inventor. That system was designed to demonstrate a capability that would greatly assist airplane accident investigators in their determination of the cause of such accidents. The FMS was the first in the world to include both Cockpit Voice and Flight Data recording. An equivalent present-day device is normally referred to as a Black Box. Such Black Boxes are almost universally regarded as electrical items although there are some non-electrical survivability aspects.

Two versions of the FMS were flight-tested, one in 1958 and the other in 1962. The purpose of this document is to provide circuit descriptions and associated analyses of the complete 1962 FMS within a single file. The FMS comprised three main items: magnetic wire recorder, airborne signal processor and ground station processor. Deficiencies in available electrical circuits for the first two items complicated the production of this document, particularly as the author is the only living person who had made a major contribution to the FMS. These deficiencies were accounted for by the author's substitution of on-paper design of circuits that could have met the requirements in 1962. Mathematical analyses of various items are included where appropriate to either enable unknown circuit values to be calculated or to assist in the understanding of the operation of some elements.

Analogue and digital presentation of the results from the 23 March 1962 successful flight validation test of the FMS are included in this document.

Contents

About the Author

The author, Mr Kenneth Francis Fraser, graduated from the University of Melbourne (Australia) in 1958 with Second Class Honours in a four-year Bachelor of Electrical Engineering (BEE) degree. There were 33 students in the final year and there was one First Class recipient, three Second Class recipients, and the author does not recall how many Third Class recipients there were. The author was ranked third in the Honours list. In third year the author received the Exhibition (ranked first) in Engineering Design for which there was a small monetary award.

At the end of the third year of the BEE degree course, the author was employed for some months as a vacation student at the Aeronautical Research Laboratories (ARL) at Fishermans Bend (a suburb of Melbourne). At the time, ARL was part of the Commonwealth Department of Supply (in 1974 ARL was shifted to Department of Defence). Later changes have resulted in the ARL name no longer being in use. The author was impressed with the type of work and the working conditions, and sought (by phone contact with the supervising scientist for whom he reported to during vacation employment) to gain employment after graduation in 1958.

Early in 1959 the author was in contact with the supervising scientist who indicated, to the author's surprise, that he had managed to recruit two assistants for him and he could now report for duty. So it was that he commenced duties (without a formal scientific suitability interview) in February 1959. At that time the graduate scientific staff were in Experimental or Scientific Officer grades. To gain entry to the Scientific Officer grade required either a PhD or a Bachelor's Degree with at least a Second Class Honour. The author thus met the minimum requirement for Scientific Officer grade. Later the Scientific Officer term was changed to Research Scientist. The author progressed through the ranks to Principal Research Scientist and retired in 2002 at age 65. Soon after the author's retirement, the Research Scientist and Experimental Officer grades were abolished and scientific staff progressed through a single stream based on performance.

After retiring the author extended his interest in computer programming, as a leisure activity, by becoming more proficient in C++ and Java computing languages. He applied these in the generation of software to solve Rubik's style cubes of large size. In 2010 he made those programs publicly available by the creation of a website www.kenblackbox.com. Some further developments since 2010 were believed by the author to be the most advanced in the world when they were made publicly available. Of particular significance was the software extensions for implementing and solving cubes with marked centres (super-cubes) over a wide cube-size range.

His website included some background on selected scientific achievements during his employment throughout the 1959-2002 period. Of particular significance was his work relating to the ARL Flight Memory (Black Box) which was the invention of Dr David Warren with whom the author had a close working relationship. The author has attempted to keep an up-to-date listing of Flight Memory items (documents, films, events, photographs etc.) in the one place (refer to www.kenblackbox.com/blackbox.htm) and there would appear to be an endless procession of such items.

The motivation to report on the electrical aspects of the Flight Memory system was a request to do that by a close friend who has agreed to maintain the above-mentioned website when the author is no longer able to do that.

Main Text

Part A: Start Items

1. Introduction

Dr David Ronald de Mey Warren (20 March 1925 – 19 July 2010) was an Australian scientist, widely recognised as the inventor of the aircraft Black Box accident recorder which comprises a Cockpit Voice Recorder (CVR) and a Flight Data Recorder (FDR). He called his invention "Flight Memory". The term *black box* generally refers to a complex system or device whose internal workings are hidden or not readily understood. The Black Box label for aircraft accident recorders was introduced by a journalist and has since been widely adopted for general public recognition, not only for aircraft but other transport systems as well.

Dr Warren was a combustion and fuels specialist. He was employed as a research scientist at the Aeronautical Research Laboratories (ARL) in Melbourne. At that time ARL was a branch of the Commonwealth Department of Supply. In 1974 ARL became part of the Department of Defence. In the mid-1950's Dr Warren was involved in the accident investigations related to the mysterious crash of the world's first jet-powered commercial aircraft, the Comet. It occurred to Dr Warren that it would be extremely useful if there had been a recording of what had happened in the aeroplane immediately prior to the crash. Dr Warren then recalled the world's first miniature recorder that he had recently seen at a trade fair. He could visualise such a recorder placed in all aircraft, continually recording details and able to be recovered after a crash.

The reason why Dr Warren's expertise was sought for the Comet crash investigations was because of his combustion knowledge – could there have been an in-flight fire? Most people would consider the aircraft Black Box to be an electrical device. That in the main is true but there are other important structural elements such as design to withstand fire, impact and water immersion. The fire proofing was one that Dr Warren was endowed with the specialist skill to achieve.

While Dr Warren was a very smart user of electrical or electronic devices, he needed electrical specialists to develop airborne recording and ground station recovery systems to validate the invention and show the results. The main aim of this document is to describe the electrical systems used in the 23 March 1962 system flight test. Many aspects of the design have never previously been documented and the author does not have complete details.

All Flight Memory system items with electrical input or output will be examined in this document. Most are electronic (using semiconductor diodes and transistors) but non-electronic electrically-related items including a motor, a battery-pack, transformers, relays, microphones, a lamp, transducers etc. will also be examined

2. Invention History

Dr Warren's earliest involvement in aircraft accident recording was in 1953 and his idea was documented (Ref. 1) in April 1954. In 1998 Dr Warren and the author produced a document (Ref. 2) that provided a brief summary of the invention and its in-flight validation.

In 1958 Dr Warren reported (Ref. 3) on extensive cockpit microphone tests he had undertaken (probably in 1957) on Vickers Viscount and Douglas DC-6B planes under arrangements provided by the Department of Civil Aviation. He concluded that good intelligibility could be achieved with optimum microphone choice and placement, and using noise cancelling arrangements.

In 1958 a magnetic wire recorder was built by instrument maker Mr Tych Mirfield under a Commonwealth Government contract arranged by Dr Warren. The magnetisable steel wire had 0.05 mm diameter and was the same as that used in the German Minifon miniature audio recorder. The ARL recorder was fully automatic for fit-and-forget operation with a "memory" mechanism that would store four hours of pilot voice and eight instrument readings at the rate of four per second up to the moment of any accident, but would automatically erase older recording for the wire to be re-used. Wire rather than tape was chosen by Dr Warren because of its compact size and its ability to withstand much higher temperatures than tape. Dr Warren claimed that this system (let us call it Mk 1) was successfully flight tested in 1958. However, the overall design was fairly rudimentary and in some respects its performance was deficient. There appears to be a lack of documentation on the electrical circuits used and the results of the flight test.

With the Mk 1 recorder on-hand in 1958, the lack-of-interest stalemate was finally broken in that year when the Secretary of the UK Air Registration Board, Sir Robert Hardingham, happened to see the recorder while on an informal visit to ARL. His enthusiasm was instantaneous. He arranged for Dr Warren to take the recorder to England to demonstrate it. The response to the demonstration in the UK was most encouraging. The BBC featured the recorder on evening television and Radio Newsreel. Many UK manufacturers and operators offered their support, and the British authorities began a move to make recorders mandatory in British civil aircraft.

Progress in Australia had to wait until the unexplained crash of a Fokker Friendship in Mackay, Queensland, in June 1960. The judge inquiring into the mysterious crash was told of the development of the ARL crash recorder and, as a result, made a judicial order that all Australian airliners must carry recorders for pilot speech as from January 1963.

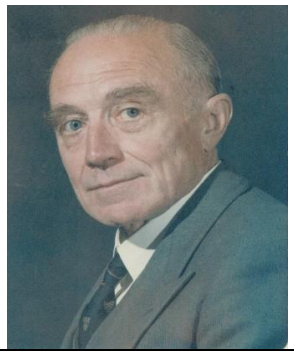
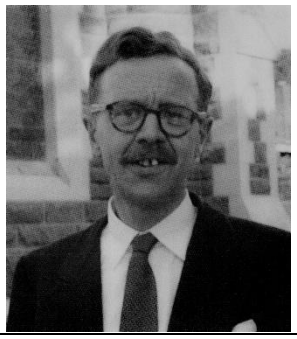
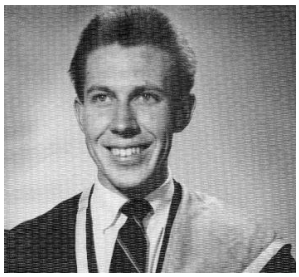
In view of renewed interest in crash recording Dr Warren who worked in the Mechanical Engineering Division of ARL sought the help of electrical/electronic specialists from the Aerodynamics Division to design and build an updated pre-production version of the recording and recovery system with improved performance (let us call the updated version Mk 2).

The involvement of the author (together with two other electrical development staff) for the Mk 2 system development began in early 1961. Details of that development form the major element of this document.

3. Overview of Flight Memory System and Participants

The block schema of Fig. 1 shows the *ARL Flight Memory System 1962* comprises three major electrical sub-systems. These are the *Recorder Unit* and the *Electronics Unit* which form the on-aircraft data recording system and the on-ground *Ground Unit* for data recovery. The *Support Equipment* is considered external to the Flight Memory system. It provides recorded signal input and processed signal output for the *Ground Unit*. The major contributors and their

involvement in the 1962 system are explained below. The photographs are those taken as close as practical to 1962.

Dr David Ronald De Mey Warren: 1925 – 2010 Dr Warren is widely recognised internationally as inventor of the black box which has a close resemblance to today's boxes. He first published his idea in April 1954. He was a combustion and fuels scientist and a very smart user of electrical devices. He organised the development and production of the recording deck for the 1962 airborne system. He designed the fireproof, impact-proof and waterproof housing for the in-flight recorder. In the workplace he was called Dave.	
Mr Tych Mirfield (Theon Numa Mirfield at birth): : 1902 – 1972 Mr Mirfield was a smart private-enterprise instrument maker who, under an ARL contract raised by Dr Warren, built the magnetic wire recording deck to meet a requirement specified by Dr Warren. Photo was taken in 1965.	
Mr Walter Francis Lane Sear: 1916 – 1983 Mr Sear was an experienced and talented electrical systems developer. In 1961-62 his contributions were the design of the signal processor which represented two thirds of the airborne *Electronics Unit*, and the audio filter which was copied for the *Ground Unit* and represented a significant contribution to that design. In the workplace he was called Lane.	
Mr Kenneth Francis Fraser: 1937 – Mr Fraser was the youngest of the 1961-62 development team His contribution to the airborne *Electronics Unit* was the design of the power system with the main item being provision of power for the *Recorder Unit*. He designed the flight data recovery system for the *Ground Unit*. His overall contribution was one third of the airborne *Electronics Unit* and most of the *Ground Unit*. In the workplace he was called Ken.	

Mr Walter Ernest Boswell: 1923 – 1989 Mr Boswell was an experienced and talented technician. In 1961-62 he created the circuit boards containing the individual electronic components for both the airborne *Electronics Unit* and the *Ground Station Unit*. That was at a time before printed circuits were in common use. He used a standard case for the airborne *Electronics Unit* and designed the case for the *Ground Unit*. He also performed the inter-wiring between the boards and the cases in which they resided. In the workplace he was called Wally.	

All personnel mentioned above except Mr Mirfield were employed at the Aeronautical Research Laboratories as it was known in 1962. While the Flight Memory project had its share of detractors in 1962, it was strongly supported by Sir Lawrence Coombes (the head of the Laboratories) and Mr Tom Keeble (the head of the Mechanical Engineering Division).

Part B: Airborne System Signal Recording

4. Airborne System

The Airborne System comprises two major hardware units: the magnetic wire Recorder and the Electronics Unit. The latter processes Cockpit Voice and Flight Data. To improve the chance of recovery of the important recorded data after an aircraft accident, it was proposed that the place where the Recorder was located should be carefully chosen (the tail being the most likely location). Recovery of the Electronics Unit after an accident would not be required and so there would not be any restriction on where it could be placed.

4.1 Recorder

The Recorder comprised mechanical, electro-mechanical and electrical components. The author could not find any electrical circuit details for the recorder except for the motor power circuit which will be examined in Sec. 4.3.

4.1.1 General

The recorder used magnetisable steel wire of 0.05 mm diameter (about the size of a human hair) as the recording medium. Magnetic wire recording was in use before magnetic tape recording which became commercially available in the 1950s. The use of magnetic wire was supported by the availability of the German Minifon P55 Type S miniature wire recorder (Fig. 2) which used a nominal wire speed of 13.4 inch per second. An advantage of wire in this application was that it could withstand a higher temperature over a given period of time than magnetic tape and storage capacity per unit volume of storage medium was very good. Disadvantages of wire include that it is single track, there is no capstan to keep wire speed constant as the wire is pulled past the head by the driving spool, and the only way to repair a broken wire is to tie the broken ends in a knot. Another reason for using wire recording was that a miniature tape recorder with the required recording duration was not available when the first ARL recorder was built prior to the 1958 flight test.

Two versions of the ARL Flight M Memory Recorder were produced. The author will refer to these as Mk 1 and MK 2 recorders. The Mk 1 was used in a flight test in 1958 (Ref. 3) and the MK 2 was used in the 1962 flight test (Ref. 2). Photographs of these recorders are shown in Fig. 3. These photographs were taken from opposite sides for the two versions of the recorder. The author does not have photographs of both sides of these recorders for either version.

Insufficient details on the Mk 1 recorder are available to the author. According to the design requirement for the recorder (Ref. 3 p13), the recorder was to be powered by “A 24V dry cell of sufficient capacity to run the recorder for 5 – 30 minutes”. If that proposal were applied, a brush-requiring DC motor would have been used.

The construction of the Mk 2 Recorder was more robust than that of the Mk 1. A photograph of the Mk 2 Recorder partially inserted into its fire-proof and impact-proof case is shown in Fig. 4. It uses a brush-less four-pole hysteresis motor designed to run from three-phase 400 Hz power, which is available as standard from aircraft inverters. Hysteresis motors run at synchronous speed which equals supply power frequency divided by half the number of poles. It was known that the required speed of the motor was 1200 RPM. Hence the motor would have to run at 200 Hz if powered from standard aircraft AC power. Except for the different

motors, the author believes the remainder of the recording unit for the Mk 1 and Mk 2 versions to be similar. The airborne systems comprise mechanical, electro-mechanical and electrical elements.

4.1.2 Magnetic Wire Movement

The basic requirement of the recorder as envisaged by Dr Warren on 8-Aug-1958 was that it would record in a continuous loop erasing just before recording. An innovative mechanism (Fig. 5) was required to meet this requirement. The author believes that mechanism with some minor modifications would have been used in both Mk 1 and Mk 2 Recorders. Electrical components are clearly visible (Fig. 5) on the lower panel for the Mk 1 Recorder. Whether batteries are also present is unclear. There is no lower panel for the Mk 2 Recorder. The recording duration for the Mk 2 Recorder was four hours.

The design of the ingenious mechanical mechanism relating to the movement of the magnetic recording wire is a significant achievement for Dr Warren and Mr Mirfield. The magnetic wire movement will be described here in three parts: Spool Rotation, Wire Stacking and End-Of-Wire Detection.

Spool Rotation

The rotational arrangement is illustrated in the top figure of Fig. 5 (which is a copy of Figure 13 in Ref. 3). The top pair of spools are designated as Set A and the bottom pair as Set B. At any time one spool is locked onto its motor-driven central shaft and drives all spools. Rotation markings in Fig. 5 are for the left Set A spool as the driver spool for which its wire is in recording mode. All spools except the driver spool move freely about their central shaft. When the Set B spools are in recording mode all the arrows in Fig. 5 are reversed with the Set B left spool now locked onto its central shaft for which its direction of rotation remains unchanged.

Wire Stacking

The stacking of the wire onto the driving spool and unstacking it from the take-up spool is a complication not applicable to magnetic tape recording. The stacking arrangement is depicted in the bottom figure of Fig. 5. The panel on which the head sets are mounted moves up and down relative to the spool sets so that the wire is always correctly aligned with the heads. Think of each layer as being similar to a tightly compressed linear spring with helical coil.

End-Of-Wire Detection

The End-Of-Wire trip switches are depicted in the bottom figure of Fig. 5. The switches are located in the right-hand spools. It is assumed that the trip-switches are mechanically-operated electrical-input on/off switches. The switches appear to be closed when wire in on the spools but are momentarily opened at the end of the reel when not held closed with wire. The author has no details on these switches. Switch possibilities include an identical switch to that used in the Minifon wire recorder and a specially made switch by Mr Mirfield. The switches may have been spring-loaded.

4.1.3 Electrical Elements

The AC motor has been mentioned above and will be examined further in Sec. 4.3 relating to the Airborne Power System. Electrical circuits relating to erase-head erasing and record-head

signal recording will be included in Sec. 4.2.2.1.3.2 Combined Signal Recording. The main item to be considered here is the provision of the clutch control signals.

The author has no electrical circuit diagram for either the Mk 1 or the Mk 2 Recorder. In a Minute written on 8 August 1958 "assistance with the [Mk 1] electrical system design by Mr W.G. Cadzow" (deceased), an ARL employee, was recognised. Mr Cadzow proposed to write a Technical Memorandum on his contribution titled "Transistorised flight data and speech equipment for a crash recorder". It has been confirmed that the proposed document was never published.

According to the Design Considerations (Ref. 3 p 11) for the Mk 1 Recorder, the use of "a two-sided magnetic clutch between the spools" is recommended and "it can be operated by a simple end-of-wire trip switch". It is assumed that the trip-switches are mechanically-operated electrical-input on/off switches. It is known (Fig. 5) that the clutches are magnetic. Whether to use permanent magnets or electro magnets would have been the first consideration. The author believes the electro-magnet option would have been chosen as that approach would render the clutches more readily controllable. Control would be by electrical input. Because the trip-switches would be off only momentarily a means would need to have been provided to hold each clutch active for a full cycle (2 hours) and then inactive for the next 2-hour-cycle.

The circuit of Fig. 6 is a hypothetical one drawn by the author to do what he believes was needed to meet the recorder's electrical requirements.

Circuit power is derived from the E_C input. Normally E_C is equal to the aircraft DC supply voltage (nominally 28 V) but under the very rare possibility of aircraft DC power failure the Flight Memory emergency battery (24 V nominal) would apply. The Power Switch Controller (Sec. 4.3.2) provides details on the Flight Memory System power switching.

The bistable flip-flop which can be triggered on and off is an obvious choice for use in this application.

A miniature solenoid-operated one-pole changeover switch is shown. Its contacts would have been required to have the capacity to pass the current required for the clutches. The magnitude of that current is not known by the author.

4.2 Cockpit Voice and Flight Data Handler

This handler comprises all the Flight Memory electrical system with the exception of the Recorder Unit which was described in Sec. 4.1. With the exception of the Power System there was no other portion of the handler that has been documented previously. A block schema of the Airborne Flight Memory System is shown in Fig. 7. Mr Sear developed the Signal Processor and the author developed the Power System.

4.2.1 External Inputs for Electronics Unit

The External Inputs comprise the Cockpit Microphone, six Transducers and the aircraft 28 V DC supply.

Cockpit Microphone

The author does not know what microphone (or microphones) were used for the 23-March-1962 flight test. The selection of microphone and placement was done by Dr Warren. He had performed extensive microphone tests (Ref. 3) in1958. In those tests he concluded that a highly directional microphone to

reduce the impact of extraneous noise sources was required. He concluded velocity type microphones provided better directional performance than pressure types because of their dependence on velocity rather than the pressure of air molecules. The author concluded that a velocity type microphone was probably used.

Transducers

For the 1962 test flight six channels were allocated for aircraft parameter recording but only five were used as indicated in the following table.

Channel Number	Parameter
3	Altitude (ALT)
4	Indicated airspeed (IAS)
5	Pitch
6	Roll
7	Cabin pressure
8	Spare (unused)

Ch 1 and Ch 2 were set at fixed voltages within the Airborne Electronics Unit.

A diagram of the transducer system is provided in Fig. 8. The author does not have Make/Model details of the transducers or their associated signal conditioners, including whether they represented a special installations for the test flight (or tapped onto standard aircraft installations). All transducer output signals were constrained to the 0 to 5 V range. The signal conditioners had to accommodate static or slowly changing parameters. Transducer arrangements for the test flight were the responsibility of Mr Don Edwards (deceased) who was a very capable and experienced technical specialist in the transducer field. He was present on the test flight.

Aircraft DC Supply

Under normal operating conditions power for the complete Flight Memory system would have been derived from the standard 28 VDC aircraft supply. Details on its use is provided in Sec. 4.3 Power System.

4.2.2 Electronics Unit

The Electronics Unit comprises (Fig. 7) two major sections, the Signal Processor developed by Mr Sear and the Power System developed by the author. Mr Boswell performed the circuit layout and assembly, and designed the case to house the electronics. A photograph of the Electronics Unit in its case beside the Recorder is shown in Fig. 9. This photograph is of poor quality but is the only one that the author has which carries the Electronics Unit label. A photograph of the Electronics Unit out of its case beside the Recorder is shown in Fig. 10. It bears the sole label ARL Flight Memory which, without the addition of "Electronics Unit" is unfortunate as the Flight Memory system also includes its inputs (cockpit microphone and transducers) and the Recorder to which its output is connected, and the Ground Station Unit.

Descriptions of the Signal Processor and Power Supply sub-sections (Sec. 4.2.2.1 and Sec 4.3) of the Electronics Unit will follow.

4.2.2.1 Signal Processor

The Signal Processor comprises all the elements within the main rectangle in Fig. 7 except the Power System which will be considered later. It has been divided into three sub-sections: Cockpit Voice Signal Processor, Flight Data Signal Processor, and Cockpit Voice and Flight

Data Combination for Recorder (Refer to Sec. 4.2.2.1.1, Sec. 4.2.2.1.2 and Sec. 4.2.2.1.3 respectively).

4.2.2.1.1 Cockpit Voice Signal Processor

The Cockpit Voice Signal Processor comprises (Fig. 7) the Pre-Amplifier, High Pass Filter, Clipper and Low Pass Filter. The High Pass Filter and the Low Pass Filter will be considered together as a Band Pass Filter. The Clipper has no effect for normal voice levels and will be considered separately.

4.2.2.1.1.1 Pre-Amplifier

The author does not have circuit details for this pre-amplifier. It would have been a multi-stage transistor AC amplifier capable of amplifying an input of some millivolts from the microphone to an output in the volt range. Nearly all amplifiers use feedback to stabilise their overall gain. Detailed analysis of amplifiers is not simple. Some further notes on amplifiers and references to documents that provide more detailed analyses of their operation are provided in Appendix 1.

4.2.2.1.1.2 Band-Pass Filter

The design requirement for the Band Pass filter was that the upper limit of its pass band be well clear of the Flight Data signal comprising switched bursts of a 3500 Hz sinusoidal signal. The setting of the lower limit of the pass band was somewhat arbitrary but had to be not too high to compromise voice intelligibility. It was also advantageous to attenuate frequencies below about 400 hertz to reduce the amount of aircraft noise which is accentuated at the low frequency end of the spectrum. Cut-off frequencies for the band-pass filter were 400 Hz and 2400 Hz. At the cut-off frequencies, the response is 3 db below that at the mid-band frequency. At 3 db, power is half and voltage is $1/\sqrt{2}$ (0.7071) of that at mid-band frequency. The ratio of upper to lower cut-off frequencies F_U/F_L equals 6.0. To achieve that separation a High Pass filter (400 Hz cut-off frequency) and Low Pass filter (2400 Hz cut-off frequency) were required. Which filter is placed closer to the microphone input is insignificant.

Basic high pass and low pass filters using R (Resistor) and C (Capacitor) components are shown in Fig. 11. Such arrangements, often with amplifier elements as well, are the most commonly used for filters. The key property of capacitors is that they block DC and lower frequency signals but pass high frequency signals readily (i.e. have frequency dependent impedance). Observe how the position of the R and C components are reversed (Fig. 11) for high versus low pass filters. Further information on the characteristics of basic electronic filters including pass band gain, cut-off frequency, phase shift and stop band attenuation slope, is readily available on the web. One such source provides relevant information for a Passive High Pass Filter (Ref. 4), an Active High Pass Filter (Ref. 5), a Passive Low Pass Filter (Ref. 6) and an Active Low Pass Filter (Ref. 7).

Although the circuit and function details for the Airborne Electronics Unit were never documented the author used the same High Pass and Low Pass Filter circuits for the Ground Station Unit and that was documented (Ref. 8). The High Pass Filter circuit (Fig. 12) is a copy of Figure 9 of the Ground Station document. The Low Pass Filter circuit (Fig. 13) is a copy of Figure 10, and the Band Pass Filter frequency response (Fig. 14) is a copy of Figure 11. For

both circuits, capacitor values are indicated in picoFarad (10^{-12} Farad) units where K $\equiv$ 10^3 . In more recent times, a 100 K capacitor, for example, would be designated as $0.1\ \mu F$.

The High Pass and Low Pass Filters for the Flight Memory project comprised standard filter circuits which included potentiometers to allow the filters' frequency responses to be adjusted experimentally. Inclusion of the basic R and C circuits is readily observed in the final circuits.

Approximate stop band attenuation slopes in the region below the 3 db cut-off frequency (from about 6 db down) have been deduced in Appendix 2 from the frequency response graph of Fig. 14. The estimate is 39 db per octave for the High Pass Filter and 46 db per octave for the Low Pass Filter. Those figures are indicative of a very high-grade band pass filter.

From the Fig. 14 graph, the attenuation at 3500 Hz (used for the Flight Data Processor) is about 30 db (a factor of 31.6 below the audio filter mid-band 0 db value).

4.2.2.1.1.3 Clipper

The author has no details on the circuit that was used to limit the voltage input to the Low Pass Filter (refer to Fig. 7). A sample clipper circuit using Zener diodes is shown in Fig. 15. Clippers are used in many applications and there is nothing special about their use in audio applications. Sound at normal levels is not affected. A Zener diode is a silicon semiconductor device that permits current to flow in either a forward or reverse direction. It has a well-defined reverse-breakdown voltage, at which it starts conducting current, and continues operating continuously in the reverse-bias mode. At the time of the Flight Memory System development Zener diodes were in common use and the author used them as voltage references for the regulated DC supplies for the Airborne Electronics Unit.

For the Fig. 15 clipper the positive clip voltage is the reverse breakdown voltage for ZD_1 plus the forward voltage drop across ZD_2 (typically about 0.7 V). The inverse applies for the negative clip voltage. Normally ZD_1 and ZD_2 would be identical. In that case, if the breakdown voltage for ZD_1 is V_B and its forward voltage drop is V_F, then the upward clip voltage would be + (V_B + V_F) and the downward clip voltage would be

(V_B + V_F). There may be a need to adjust V_{IN} (by a suitably chosen voltage divider for instance) if Zener diodes of desired breakdown voltage are not available.

4.2.2.1.2 Flight Data Signal Processor

The author has notes on various configurations for the Flight Data Signal Processor that reveal some minor differences. The configuration that will be adopted in this document is that for which the most information is available. The Flight Data Signal Processor comprises (Fig. 7) the Clock Pulse Generator, Multiplexer, Analog Output Offset Producer, Pulse Duration Modulator, and Sine-Wave Amplitude Modulator.

4.2.2.1.2.1 Clock Pulse Generator

The author does not have circuit details for the 24 Hz Clock Pulse Generator (refer to Fig. 7). For the Airborne Electronics Unit Power System (Sed. 4.3) the author had used an RC circuit, unijunction transistor and divide-by-two flip-flop to obtain a rectangular output with equal duration up and down levels. Although the circuit used was for a different frequency output, the requirement for the Clock Pulse Generator was otherwise the same. The circuit shown in

Fig. 16 provides component details for a 24 Hz output signal equivalent to the circuit (Fig. 41) for the 400 Hz output signal used in the Power System except for the capacitor with a different capacitance value.

Adding the suffix 1 to designate the values for the R_1 and C components and the output signal frequency for the 400 Hz version, and suffix 2 for the 24 Hz output version, then if R_{12} equals R_{11} it follows that $C_2 = \frac{C_1 f_1}{C_2 f_2}$. For the 400 Hz version C_1 equals 0.12 µF, and that gives (C_2 = 2.0 µF). The value R_1 (Fig. 16) equals 18 K is nominal and needs to be trimmed experimentally to provide the 24 Hz signal output. For the 400 Hz version that was achieved using a fixed 15 K resistor in series with an adjustable 5 K resistance trimmer.

The author had some notes on an alternative circuit arrangement that would provide reference signals 24 Hz and 3500 Hz (approximately) from a common source. Details are provided in Appendix 3. The 3500 Hz is required for the Sine-wave Amplitude Modulator (Fig. 7). While the circuit would provide the 24 Hz clock frequency, the carrier frequency for the Amplitude Modulator would be 3456 Hz, slightly less (1%) than the 3500 Hz design value. That difference would be hardly noticeable.

4.2.2.1.2.2 Multiplexer

The Multiplexer circuit shown in Fig. 17 is based on the author's undated hand-written notes. The circuit comprises three semiconductor integrated-circuit components (Q_1, Q_2 and Q_3) and a few discrete components. Q_1 (SN5470) is a positive-edge-triggered Flip-flop with Preset and Clear. It divides the input clock frequency by 2. Q_3 and Q_4 (both MM454F) are four-channel multiplexers with Q_2 handling odd channels (1, 3, 5 and 7) and Q_3 handling even channels (2, 4, 6 and 8).

The author is not sure this circuit was used in the Flight Data Processor and was unable to confirm that. SN5470 and MM454F integrated-circuit types were available in 1961 when the Mk 2 Flight Memory system was being developed.

4.2.2.1.2.3 Analog Output Offset Producer

If the 5 V transducer output is represented by 100%, then the following apply:

Input	Output
5.5 V MARKER (Fig. 7)	120%
5 V transducer output	110%
0 V transducer output	10%

The Analog Output Offset Producer has two purposes:

- Produce a zero-offset equivalent to 10% of the full scale (5.0 V transducer output) if the zero offset in the PDM is set to zero volt.
- Produce a 10% over-limit to accommodate the MARKER (used mainly for channel synchronization during Ground Station Flight Data recovery). That would mean producing 5.0 V output for a 6.0 V input if the zero offset in the PDM were set to zero volt, or to producing 5.0 V output for a 5.5 V input if the zero offset were performed in the PDM.

The required zero offset can be provided as detailed here or via the adjustment available in the PDM. In either case there is a need to limit the PDM input signal to 5 V maximum. An analysis of an emf (electromotive force) and resistor network that would be suitable for producing the required analogue voltage input to the PDM is provided in Appendix 4. By setting the zero-adjustment-leg open-circuit, the zero-adjustment-within-the-PDM option can be adopted.

4.2.2.1.2.4 Pulse Duration Modulator (PDM)

Overview

The Flight Memory PDM circuit is based on a 1958 Electronics Engineering article (Ref. 9) for a Telemetry Keyer which used a sampling rate of 900 readings per second and a signal input range of 0 to 5 V. That meant some changes were required for the Flight Memory application which used a 24 readings per second sampling rate and a nominal 5.5 V analogue input signal range (if the zero-signal offset were included in the PDM circuit). In the document currently being written, PDM is used in lieu of Keyer as that terminology better describes its function and is more recognizable by the electrical engineering and scientific communities. There is no record available (to the author) on what changes were incorporated. Fig. 18 is a block schema of the PDM and it is valid for both 900 and 24 Hz versions. Circuit details for the 1958 Telemetry Keyer are provided in Fig. 19. While most of the important components had labels (e.g. Q_1 to Q_8 for transistors, R_2 etc. for some resistors and C_1 etc. for some capacitors), other components were unlabelled. To facilitate the functional description of the PDM's operation, labels have been added to all those components that did not have them in the original circuit. C_1, which was used for two different components in the original circuit, has been expanded to C_1 and C_2.

There is no written record of the Flight Memory PDM circuit. The author can confirm that all transistors are the same as those used in the 900 Hz version. All diodes, except D_3 and D_1 (both SV122 Zener diodes), are silicon types which, when conducting, will have a nominal voltage drop of 0.7 V. The author could not find any details on D_3 and it is assumed that device is no longer in production. According to Ref. 9, "Zener diode D_3 is used for a 5 V reference". It is assumed that it is a 5.1 V Zener diode (standard type available) that will clip any input signal in excess of 5.8 V (adding D_3 and D_4 voltage drops). Use of D_3 would be unsuitable for an input signal in excess of 5 V.

The required pulse width output for the Flight Memory System is known from the settings for the Sine-Wave Amplitude Modulator (Fig. 7) to be reviewed in a later Section. The required pulse durations are indicated in the following table.

Analog input	Number of 3500 Hz cycles	Pulse duration (msec)
0 V transducer minimum	10	2.86
5 V transducer maximum	110	30.56
5.5 V MARKER channel	120	34.29

The period of the 24 Hz Timer (Clock) input is 1/24 sec which equals 41.67 msec. That provides a minimum gap of 7.38 msec or 17.7% of the Timer (Clock) period.

The block schema (Fig. 18) indicates the modulator comprises four distinct elements:

1	Trigger Delay
2	Bootstrap Ramp Generator
3	Voltage Comparator
4	Bistable Flip-Flop

While element 1 has no input from the three other elements, elementss 2, 3 and 4 are very much inter-related. These elements will be examined next, mainly in terms of what does and what does not need to be changed relative to the 900 Hz Keyer.

Trigger Delay

The purpose of the Trigger Delay circuit is to provide a delay from the time at which the multiplexer switches to a new channel to the time at which the analogue input is interrogated. This ensures the analogue input has stabilised before its value is measured. The Trigger Delay circuit comprises Q_1, Q_2 and associated components (in Fig. 19).

For zero signal from the Timer Q_1 is saturated and Q_2 is drawing no emitter current. If a negative-going gate is applied from the Timer input, Q_1 is driven to cut-off allowing capacitor C to charge. As its voltage rises so does the voltage on the delay-adjustment resistor R_2. At a certain instant emitter current will be drawn from the unijunction transistor Q_2. As the emitter of Q_2 draws current the base current of Q_2 drops very rapidly and its emitter voltage drops to zero.

The input impedance of Q_1 is low (42 ohm approximately). Hence for zero signal in, the base current of Q_1 is about 24/75 mA (0.32 mA).

Analysis of the operation of the Trigger Delay circuit is much more complex than those for the other three PDM elements. The author found some of his hand-written notes (undated but probably written in 1961) on the derivation of the magnitude of the time delay. A copy of that analysis with some extensions is provided in Appendix 5.

The Appendix 5 analysis determined that about 60% adjustment of the R_{V4} potentiometer provided trigger delay adjustment in the approximate range $(0 \text{ to } 211\ \mu s)$. For the remaining 40% adjustment of R, unijunction transistor Q_2 will be switched on and its emitter grounded (0 V). Ref. 9 indicated that 100 μs delay was used for the 1958 Telemetry Keyer. That value should also have been suitable for the Flight Memory PDM as the analogue input stabilisation time is mainly a function of such times for the Flight Data Processor's switching devices and external transducers. These times would be similar for the 900 Hz Keyer and the 24 Hz Flight Memory applications.

Bootstrap Ramp Generator

A perfect ramp generator is one for which its slope is constant over the period of interest. The voltage versus time and current relationship for a capacitor is well known. It is given by:

$$\frac{dv}{dt} = \frac{i}{C}$$

where C is the capacitor's capacitance in Farad, i is the instantaneous current through the capacitor in Amp and $\frac{dv}{dt}$ is the instantaneous rate of voltage change (volt per second). By

creating a circuit which sets i constant, the requirement to set $\frac{dv}{dt}$ constant would be achieved. To highlight the constant current, the instantaneous i in the above equation will be replaced with capital I as shown below.

$$\frac{dv}{dt} = \frac{I}{C}$$

The actual ramp generator circuit is shown in Fig. 20A and simplified equivalent circuits for without and with internal zero offset are shown in Fig. 20B and Fig. 20C respectively. A zero offset is essential and hence Fig. 20B is applicable where the zero offset is arranged external to the PDM. Arranging the zero-offset external to the PDM is the simpler approach particularly as there is a need to restrict the maximum input signal to no greater than 5V and adding the zero-offset adds no extra complexity as indicated in Sec. 4.2.2.1.2.3.

Irrespective of which zero offset option is used, the PDM output pulse duration will be equal to the ramp signal duration. For no internal zero offset in the PDM, ramp capacitor C_2 will be fully discharged (voltage drop across it is equal to zero) when the ramp is inactive (PDM output is high). Also, transistor Q_9 and its equivalent switch SW will be in the ON state when the PDM output is high.

Proper operation of the ramp generator requires bootstrap capacitor C_F to rapidly charge to $(V_{CC} - V_D)$, where V_D is voltage drop across diode D_2 when switch SW (Fig. 20B) is closed and retain this DC voltage drop when SW is opened. For (V_{CC} = +24V), and (V_D = 0.7V), the DC voltage drop across C_F will be 23.3V. The current into the ramp capacitor C_2 will be the current through R_A minus the base current into Q_8. As indicated in Ref. 9, the base current for Q_8 should remain constant for the duration of the ramp. For this analysis it will be assumed that the base current through Q_8 is negligible. With that assumption the current through C_2 will equal the current through R_A. For the current through R_A to be constant, the voltage drop across it must remain constant. To achieve this the AC ramp component voltage must also appear at the C_F-to-D_2 junction. As soon as the ramp voltage across C_2 begins to rise, diode D_2 will cease to pass current and bootstrap capacitor C_F will provide the current for R_A, and C_F will act as a short circuit for the AC ramp voltage which will appear at each end of C_F. The value of C_F must be large enough to retain its DC voltage drop during ramp generation but not so large that replacement of any lost charge (assumed to be small) during ramp generation cannot be rapidly achieved. A suitable value for C_F is the value used in the original keyer application multiplied by the ratio of original sampling rate to that for the Flight Memory application.

$$C_F = 8 \text{ x } (900/24)\ \mu F = 300\mu F$$

The effect of the inclusion of the zero offset will now be considered. If D_1 (Fig. 20A) were a standard silicon diode it would be reverse-biased and the voltage drop across R_{V3} would be:

$$\frac{V_{BB}\ R_{V3}}{R_9 + R_{24} + R_{V3}} = \frac{-24 \text{ x } 1000}{562 + 1210 + 1000} \text{V} = -8.66 \text{ V}$$

However, D_1 is a Zener diode with breakdown voltage of 5.1 V (presumably as indicated earlier). The above calculation verifies that the breakdown condition would apply. While the operation of the actual zero offset circuit (Fig. 20A) is difficult to comprehend, it can

be radically simplified as shown in Fig. 20C. When switch SW is closed the emitter of Q_8 will be set to $-kV_Z$ (refer to Fig. 20A) and that approximate value will also be transferred to ramp capacitor C_2. In practice, kR_{V3} would be adjusted experimentally to provide the required zero offset. The following would apply for the "Internal-to-PDM" and "External-to-PDM" zero offset options.

Zero offset option	Initial voltage across ramp capacitor C_2	Voltage across bootstrap capacitor C_8
Internal-to-PDM	$-kV_Z$	$V_{CC} - V_D + kV_Z$
External-to-PDM	0	$V_{CC} - V_D$

The next step is to calculate the required capacitance value of C_2 for the Flight Memory application. Recalling the basic relationship between ramp slope $\frac{dv}{dt}$, C_2 charging current and the C_2 capacitance value, the following applies.

$I = M$, where $\left(M = \frac{dv}{dt}\right)$ and is assumed to be constant.

Let V_X be the DC voltage drop across bootstrap capacitor C_8. It will be the same when transistor Q_8 is ON and when it is OFF. The charging current I, for ramp capacitor C_2 is given by:

$$I = \frac{V_X}{R} = MC_2$$

$$M = \frac{V_x}{RC_2}$$

The pulse duration equals the ramp duration, and assuming a perfectly linear ramp, M can be calculated for any ramp duration but it is convenient to do so for its longest duration (i.e.. for MARKER). First consider the options detailed in the following table.

PDM Internal Offset Table

Calibration	EXT OFFSET Fixed V_{ZB}	Transducer Signal Range Variable v_{TA}	INT OFFSET Fixed V_{ZA}	MARKER Fixed V_{SA}
100%	0% (None)	0% to 100%	100% to 110%	120%
4.545 V	0.00 V	0.00 to 4.545 V	0.455 V	5.00 V

PDM External Offset Table

Calibration	EXTt OFFSET Fixed V_{ZB}	Transducer Signal Range Variable v_{TB}	INT OFFSET Fixed V_{ZA}	MARKER Fixed V_{SB}
100%	10%	10% to 110%	None	120%
4.167 V	0.417 V	0.417 to 4.583 V		5.00 V

The INT and EXT Zero voltage offsets are slightly different (5.0/11 = 0.4545) versus (5.0/12 = 0.4167) respectively. The difference (5/11 – 5/12 = 5/132) represents 0.758 % of full-scale input voltage (5.0 V) difference.

The pulse duration T_S for the MARKER signal is 34.29 ms and must be the same for INT and EXT zero offset settings.

$$M = 5.00/34.29 = 0.1458 \text{ volt/ms}$$

$$M = \frac{V_x}{RC_2}$$

V_X has different values depending on whether the zero offset is performed within the PDM or external to it. Suffix A will be added for the former and B for the latter.

$V_{XA} = +V_{CC} - V_D + kV_Z = 24 - 0.70 + 0.4545 = 23.7545$ volt
$V_{XB} = +V_{CC} - V_D = 24 - 0.70 = 23.3$ volt

$(RC)_A = \frac{V_{xA}}{M} = \frac{23.7545}{0.1458} = 162.92$ ms

$(RC)_B = \frac{V_{xB}}{M} = \frac{23.3}{0.1458} = 159.81$ ms

If (R = 410 K), then $C_{2A} = 0.397$ µF and $C_{2B} = 0.389$ µF

C_A and C_B are close to being the same. Setting (C_2 = 0.39 µF) and trimming the adjustable R value to set pulse duration to its correct value, would be appropriate.

When the Zero Offset is provided internal to the PDM, the required value is V_Z, where V_Z is the breakdown voltage for Zener diode D_1 (Fig. 20A). As shown above, kV_Z equals 0.4545 V. As V_Z = 5.1 V, (k = 0.095) which is about 10% of the adjustable range for R_{V3}. Replacement of R_{V3} (1000 ohm) with 820 ohm (fixed) in series with a 200 ohm variable resistance would have been more appropriate for the Flight Memory application.

Voltage Comparator

The voltage comparator circuit is shown in Fig. 21A. It is powered from the V_{BB} (−24V) supply. It has two input signals:

1. SIG IN (Fig. 19) comprising a scale-adjusted multiplexer output plus a zero offset if the external zero offset option applies.
2. The output from the ramp generator.

For convenience the above signals have been given the designation e_S and e_R respectively.

For any multiplexer channel, it can be assumed that e_S remains constant for the full clock period (1/24 sec) and will have a maximum value of 5.0 V for the MARKER channel. The ramp generator output e_R will have a start-value of zero volt or close to that value if the internal zero offset option is in use.

The over-voltage clipper (Fig. 19) sets a clip voltage equal to the breakdown voltage of Zener diode D_3 plus the ordinary conducting voltage of silicon diode D_4. The clip voltage has been excluded from the voltage comparator considered here (Fig. 21A) as it represents an open circuit at all times for within-range e_S signals. The voltage comparator is a Schmitt

trigger circuit. For *($e_R < e_S$),* Q_6 is reverse biased (non-conducting). The input impedance loading for e_S is very high and further increased via feedback capacitor C_1. The size of this capacitor would need to follow an inverse relationship to the sampling rate. C_1 for the 900 Hz Keyer had a value of 100μμF and so a value of 3750μμF approximately would be suitable for the Flight Memory application. Q_7 is actively biased while Q_6 is switched off. For *($e_R < e_S$)*, the output of Q_7 will have a high value. When *($e_R = e_S$)* the emitter of Q_6 will become forward-biased. At that instant Q_6 will switch on and the output of Q_7 will drop sharply. The output of the voltage comparator is AC coupled via C_7 to the FLIP-FLOP and provides its Output-Pulse-End-Trigger. The 330μμF value for C_7 used for the 900 Hz Keyer should also be suitable for the Flight Memory application.

A simplified equivalent circuit for the voltage comparator is shown in Fig. 21B. It shows a high-gain inverting amplifier with relevant signal waveforms. When *($e_R < e_S$)* the output is high and when ($e_R > e_S$) it is low with an abrupt changeover when *($e_R = e_S$)*..

The table in Fig. 21C summarises the Input Signal e_S and Ramp Signal e_R voltage ranges according to whether the zero offset is performed internal-to or external-to the PDM.

Flip-Flop

The complete Flip-Flop circuit is shown in Fig. 22A. Transistors Q_3 and Q_5 are used in a conventional edge-triggered flip-f lop arrangement and Q_4 in a unity gain output amplifier. It is helpful to consider the flip-flop and the output amplifier as separate entities as indicated in Fig. 22B and Fig. 22C respectively**.**

The output amplifier connects to the flip-flop between points X_A and X_B (Fig. 22B). In that figure X_A and X_B are joined together and that is a close approximation for the effect of the output amplifier on the operation of the flip-flop. The symmetry of the flip-flop is obvious when the flip-flop is drawn as shown in Fig. 22B. ON and OFF voltage triggers are connected to the base terminals of Q_3 and Q_5 respectively via diodes which guarantee that only the negative portions of the edge triggers are received by Q_3 and Q_5. Both triggers produce momentary switch-off of Q_3 and Q_5 respectively. Reinforcement via feedback resistors R_{20} and R_{15} resistors ensure that the switch-off states of Q_3 and Q_5 respectively are maintained. The pattern of high (H) and low (L) states of Q_3 and Q_5 are summarised in the following table.

Condition	Collector Q_3	Collector Q_5
Before ON	H	L
After ON	L	H
After OFF	H	L

The output amplifier (Fig. 22C) is a Common Collector (Ref. 10) type. Its gain (emitter voltage divided by base voltage) is close to 1. Input and output voltages are in phase, input impedance is high and output impedance is low. This means there is negligible loading on the input signal source and the amplifier's output "sees" a much higher impedance than the actual load value that would apply for an amplifier without feedback stabilised gain. Final output voltage is adjustable in the range 0 to 75% of Q_4 emitter voltage via the R_{19} and R_{V1} voltage divider.

Complete PDM Circuit for Flight Memory Application

Some changes relative to the 900 Hz modulator (Fig. 19) were required for the 24 Hz Flight Memory application. No changes to semiconductor or resistor components were deemed necessary. Also, no changes were required to capacitors which performed edge triggering operations. It was necessary to change the values of three capacitors (C_2 and C_8 for the Ramp Generator, and C_1 for the Voltage Comparator). New values are ($C_1 = 3750$ μμF), ($C_2 = 0.39$ μF) and ($C_8 = 300$ μF). While the capacitor values are theoretically correct, in practice capacitor values would be trimmed experimentally to meet requirements. Circuit details for the 24 Hz Flight Memory PDM are shown in Fig. 23.

Voltage versus time graphs for one input scan cycle (eight channels) relevant to the PDM are shown in Fig. 24. The 24 Hz Clock (Timer) is shown with equal low and high periods but any other low to high ratio could be used. The essential requirement is that the high-to-low transitions are separated by exactly $\frac{1}{24}$ second. For the Flight Memory application, the ramp durations for CH 7 (Zero) and CH 8 (MARKER) are invariant. Because the MARKER duration is the duration of 120 cycles of a 3500 Hz sine-wave carrier, and the Zero is $\frac{1}{12}$ of that, it should be possible to delegate CH 1 to an additional transducer channel. The ramp durations for CH 1 to CH 6 have been set to arbitrary values in Fig. 24.

4.2.2.1.2.5 Sine-Wave Amplitude Modulator

The Sine-Wave Amplitude Modulator (Fig. 7) has a single input which is the PDM's output. It produces bursts of 3500 Hz sine-waves that coincide with the periods for which the PDM output is low. The author has no details of the electronic circuit that was used to perform this function.

What is known is that the sine-wave burst started at full amplitude as illustrated in Fig. 25A. The author is unsure of what happened at the trailing end of the burst. The author has been unable to find a reference to a circuit that would instantly reach full magnitude sine-wave oscillation on receipt of a control signal. Jimenez (Ref. 11) describes a gated oscillator which starts without delay but the oscillator is not sinusoidal.

An equivalent circuit for a Phase-Shift (RC) oscillator (Ref. 12) with gated on/off control is shown in Fig. 25B. This circuit represents a conventional method for producing a gated oscillator output. It employs a sine-wave oscillator with continuous output coupled to a gating signal input (the PDM output). While the idealized sine-wave bursts are shown in Fig. 25B, in practice there will be irregularities for the first couple of cycles and some add-on after the trailing edge of the PDM gate signal. The inherent filtering of the recording and reproducing processes will mean that the sharp transitions of the sine-wave bursts will not be retained.

Because the sine-wave bursts were not band-pass filtered prior to recording, some unwanted signals could be transferred to the audio band. Such unwanted signals will be considered in the next section.

4.2.2.1.3 Cockpit Voice and Flight Data Output Generator

This item has two elements: the Combiner and the Current Output Amplifier with the latter providing the signal that is passed to the Magnetic Wire Recording Deck. These elements are shown in the Fig. 7 block schema.

4.2.2.1.3.1 Combiner

The Combiner (Fig. 7) combines Cockpit Voice and Flight Data signals into a single output for which the two items are separated by frequency. The author has no details of the circuit that was used. A simple resistance network is the usual approach and it is assumed to be what was used. Appendix 4 and Fig. A4 provide a general analysis for an n-emf system. The analysis is simplified by using conductance in lieu of resistance. A simplified equivalent circuit is shown in Fig. 26A and the actual circuit is shown in Fig. 26B.

Defining Cockpit Voice audio input as e_A, Flight Data input as e_F and the Combiner output as e_C, the following equation applies:

$(e_C = k_1 e_A + k_2 e_F)$ where $k_1 = \frac{G_1}{G_1 + G_2 + G_3}$ and $k_2 = \frac{G_2}{G_1 + G_2 + G_3}$

If each conductance is replaced with its inverse resistance the following apply:

$$k_1 = \frac{R_2 R_3}{R_1 R_2 + R_2 R_3 + R_1 R_3} \; and \; k_2 = \frac{R_1 R_3}{R_1 R_2 + R_2 R_3 + R_1 R_3}$$

$$if \; R_1 = R_2 \; and \; R_3 \gg R_1, then \; k_1 = k_2 \cong 0.5$$

Such an approximation would apply if $(R_1 = R_2 = 15K)$ and $R_3 = 150K$.

It is assumed that the Output Amplifier (Fig. 7), to which the Combiner output is connected, has very high input impedance due to feedback (it is assumed to have unity voltage gain).

The author performed a Fourier analysis (Ref. 13 p3) of a pulsed sinusoidal voltage mainly in support of the design of the filter for the Ground Unit's Flight Data recovery. An extension of that analysis in Appendix 6 shows that the pulsed sine-wave signal e_F for the Flight Data signal has residual components within the pass-band of the Cockpit Voice signal. That combined with a small proportion of the Flight Data signal passed by the audio filter during ground system data recovery was responsible for the presence of a regular undefined audio signal (of relatively low volume) that could be heard when no voice signal was present on the recorded audio channel. The author has no record of that signal. The author likened the extraneous sound to that of the Australian Mole Cricket insect's song and that is also elaborated upon in Appendix 6. It was concluded that eliminating the problem would have been straight forward once its cause was established.

A high pass filter inserted between the Sine-Wave Amplitude Modulator and the Combiner (Fig. 7) would have resolved the problem. Since the Flight Memory Electronics system never proceeded to commercial production, no further development took place after the 23 March 1962 flight validation test. Hence the problem remained unresolved.

4.2.2.1.3.2 Combined Signal Recording

The following recording-related actions were required:

1. Provide a high frequency erase signal for the erase-head to remove any pre-recorded signal from the wire before it passes the record-head.
2. Provide a high frequency inaudible sine-wave (bias) signal to be added to the record-head signal to improve recording quality.

3. Provide record-head signal current unaffected by frequency-dependent record-head impedance.

The high frequency signal for 1 and 2 can be the same. For tape recorders it is generally in the 40 to 150 kHz range (the author used 55 kHz in a different tape-recording application – Ref. 14) and the requirement for magnetic wire recording would probably be similar. Ref. 15 has a block diagram showing the erase-head signal and the record-head bias signal as being the same, and record and playback using the same head. That arrangement matches that for the Flight Memory system recording and playback.

The author has no details for the actual circuit that was used for the Flight Memory system erasing and recording. A simplified circuit that would meet the Flight Memory recording requirement is provided in Fig. 27.

The same head was used for both airborne system input signal recording and output signal playing hack for the ground recovery system. Fortunately, the author made some measurements on the head characteristics that were relevant not only for playing back but also for recording. The relevant information is provided in Ref. 8 (Figure 3). The magnitude of the bias current was indicated as 250 μA DC (should have been indicated as AC and the author will assume it was a peak value). The AC record-current was indicated as 200 μA peak (assumed to be the 100% signal value). To obtain the required record-head signal current (i_{RH}), resistance value of R_1 would need to be made much higher than the impedance value of the record-head over the frequency range of interest (400 to 4000 Hz approximately). Capacitor C_1 would be used as a DC blocker and its impedance over the frequency range of interest would need to be much lower than the R_1 resistance value.

The record/playback head impedance as a function of frequency was plotted in Ref. 8 (Figure 4). There was a labelling error in that figure. The vertical axis marked as KILOHM should have been OHM and likewise the DC resistance should be 2.2 OHM. From the corrected figure, the record/playback head impedance at 4 KHz equals 600 ohm. If L represents the record-head inductance and f the frequency, then the record-head impedance would be equal to $2\pi fL$. Using ($2\pi fL$ = 60 ohm at 4 KHz), gives (L = 2.4 mH {milliHenry}) which is a reasonable value for a record-head inductance.

For a 100% record-head current i_{RH} of 200 μA, and for a nominal value of 5 V peak for e_c, (Fig. 27), (R_1 = 25 K) would apply. A value of 1.0 μF would be suitable for C_1.

The simplified recorder input schema (Fig. 27) shows the amplifier as a unity gain voltage type. That arrangement agrees with handwritten notes the author made around 1961, but a higher gain amplifier could have been used. The use of unity gain minimises the amplifier output impedance but, with a load of about 25 K, a very low output impedance is not a requirement. A gain stabilised amplifier by feedback is the main requirement.

The sine-wave oscillator (Fig. 27) would provide high frequency erase-head current and record-head bias current. The simplified circuit at the upper right of Fig. 27 shows an arrangement for one of the two erase-and-record head-sets.

The "Head Set Switching Circuit" (Fig. 27) shows a method of providing the required electronic circuit switch-over from one spool-set to the other. OP-A is the same signal (Fig. 6)

that operates one of the trip-switch triggered magnetic clutches for the recorder. OP-B (Fig. 6) is the inverse of OP-A and could be used if a reverse-order switching were required. A nominal 24 VDC solenoid-operated 2-pole change-over switch performs the required spool-set switch-over. When a high signal is applied, the solenoid would activate its switch and when low it would return to its inactive (opposite) switch state.

According to Dr Warren (Ref. 3 p10) who details Design Considerations for the Mk 1 Recorder, "All record of the flight would be erased during taxi-in". The author presumes a similar intention would apply for the Mk 2 Recorder. The proposed automatic erasing would be far from simple and, even if it were realizable, it would be practical for only short duration flights. The author is sure this proposal never proceeded to a test or implementation stage. Post-flight manual erasing by ground support staff would appear to be required to accommodate long duration flights.

If it could be assumed that, by some means, every new flight were to start with the spools containing fully erased magnetic wire and the spools were positioned such that recording always started where spool A was just about to engage its End-Of-Wire trip switch (Fig. 5), then a major design simplification would apply. There would not be a requirement for recording to continue from where it was at the time of the successful landing for the previous flight.

4.3 Airborne Power System

The two major requirements of the Power System were to:

- Provide DC power for the Electronics Unit, Transducers and Recorder.
- Provide AC Power for the Recorder motor.

Detailed design information for the Power System is provided in Ref. 16 which was written by the author whose responsibilities included the provision of the Airborne Power System. Complete details of the Power System design are provided in the above referenced document which is in PDF format and can be readily viewed on-line. The main aim of the following sub-sections is to provide a summary of functions, analyses and circuits for the power system.

4.3.1 Overview

At a high level ARL staff meeting (Appendix 7) it was decided that an emergency battery would be included in the airborne system to allow recording to continue if an electrical power failure occurred during flight. That decision had a major impact on the Airborne Power System development as the simplest solution was to derive both normal and power-loss-emergency power from DC sources. The chosen setup was to derive normal power from the aircraft 28 VDC supply and the emergency power from a rechargeable 24 VDC battery supply. The other standard aircraft supply (200 VAC inter-phase 400 Hz) would have provided a simpler implementation if no emergency battery back-up had been required.

A simplified block schema of the Power System is included in Fig. 7. An extended block schema of the Power System is shown in Fig. 28. The complete Power System, including the emergency battery pack, was installed in the Airborne Electronics Unit.

Three transformers were included in the power system (one in the DC output section and two in the AC output section). All transformers were designed in-house and used cores that were available at the laboratory.

Primary emf sources are given an E designation (E_A for standard aircraft 28VDC supply, E_B for the Flight Memory 24VDC emergency battery supply, and E_C for the switched output which is normally equal to E_A but in the extremely rare event of an aircraft 28VDC failure it would be equal to E_B).

4.3.2 Power Source Controller

A simplified circuit for the Controller is shown in Fig. 29a (which is a copy of Ref. 16 Figure 1). Relay switching, which provides a simple means of controlling amps (if required) of output current with milliamps of coil current, is used. Relay P1 provides single-pole-changeover switching and P2 is the same as P1 although in that case on-off switching is all that is required. The comparator (to be described below) will energise P1 if the aircraft supply voltage exceeds 21 V and will abruptly de-energise P1 if aircraft supply drops below 21 V (an indication of aircraft 28 VDC failure).

Provided switch S is closed, relay P2 will remain energised both when aircraft supply is normal and if and when aircraft power fails. Simplified circuits Fig. 29b and Fig. 29c show arrangements which would have applied for normal and emergency operation. During normal operation the diode allows charging current from the aircraft supply to pass to the battery but prevents any discharge back into the aircraft supply. If switch S is closed and the aircraft supply is switched off, the emergency battery will provide power to the recording system and hence discharge. It is therefore essential that switch S be opened after a normal landing. The general requirement that the recording system be installed on a "fit and forget" basis rules out the possible solution that the pilot manually operates switch S. One possible solution would be for switch S action be provided by a connection to the weight-on-wheels (WOW) switch in common use in relation to aircraft undercarriage operation.

The battery cells in use were Nickel-Cadmium sintered plate type with a nominal cell voltage of 1.2 V. The battery pack comprised 20 such cells giving a nominal pack voltage of 24 V.

The comparator switch shown in block form in Fig. 29a uses a Schmitt trigger circuit. The P1 and P2 relays used are miniature military-qualified type M200 manufactured by Leach Corporation. These relays are a 2-pole-changeover type with only one pole in use for the Flight Memory application. The relay contacts are rated at 2 A resistive. To energise the 600 ohm coils in these relays about 18 V maximum is required. The drop-out voltage is in the vicinity of 5 V.

The basic form of the comparator circuit is shown in Fig. 30 (which is a copy of Ref. 16 Figure 3). At low levels of input voltage V, with Zener diode V_Z not conducting, Q_1 will be "on" and Q_2 will be "off", provided that $\left(\frac{R_2}{R_1} < \frac{R_4}{R_3}\right)$. When $\left[V = \left(1 + \frac{R_3}{R_4}\right) V_Z\right]$, the Zener diode will conduct and hold the common emitter point fixed relative to the negative supply line. Q_1 will continue to conduct until reverse bias appears on its emitter-base junction. This will occur when $\left[V = \left(1 + \frac{R_1}{R_2}\right) V_Z\right]$. At this level of input voltage, the Schmitt circuit will change state, with Q_2 switching "on" and Q_1 "off". A positive going step of voltage approximately V_Z volt in magnitude will appear on the collector of Q_2. This pulse is fed via emitter follower Q_3 to transistor Q_4 which acts as a switch. The low breakdown voltage Zener diode in the emitter

circuit of Q_4 ensures that Q_4 is "off" until the "on" pulse appears. If the supply voltage drops below $\left(1 + \frac{R_1}{R_2}\right) V_Z$ the circuit switches back abruptly and the relay drops out.

The complete power system switching circuit, with component values indicated, is shown in Fig. 31 (which is a slightly modified copy of Figure 4 in Ref. 16). Adjustment of the comparator's switchover voltage is enabled with the 5 K potentiometer. For the input voltage divider values chosen $\left(0.81 < \frac{R_1}{R_2} < 1.64\right)$. Using the nominal 10 V Zener diode shown, the switchover voltage could be adjusted within the 18.1 V to 26.4 V range, with the desired 21 V about mid-range.

It was found necessary to decouple the comparator from the voltage supply input using the RC network shown at the upper left of Fig 31 to prevent relay chatter at full load when the comparator was set at the switchover voltage. Transistor Q_4 was protected from large voltage transients at switch-off by connecting a diode across the relay coil.

E_C (Fig. 31) represents the DC input power source for the Flight Memory System. In normal operation E_C equals E_A (28 V nominal) whereas in emergency battery operation E_C equals E_B (24 V nominal).

4.3.3 Provision of DC Outputs

All items in this Section have been described in detail in Ref. 16 and Ref. 17 which are in PDF format and readily viewable. Functional diagrams, some analyses and final circuits have been copied and included in this Section.

4.3.3.1 Requirement

The power requirement defined by Mr Sear was as follows:

+36 V Reg. at 25 mA

+24 V Reg. at 25 mA

−24 V Reg. at 55 mA

+5 V Reg. at 50 mA

+250 V Unreg. at 0.6 mA

The calculated total output is 3.7 volt-amp. Assuming unity power factor that translates as 3.7 watt. A design requirement of 6 watt input power was adopted.

The author has been unable to find out what the +36 V supply was used for. It was not used in the Cockpit Voice Processor or in the Flight Data Pulse Duration Modulator. The +24 V and −24 V supplies were used extensively in the Cockpit Voice and Flight Data Processors. The +5 V supply was used by the transducers. The +250 V supply was used for a power-on indicator for the Flight Memory Electronics Unit, and in view of the 0.6 mA current requirement, it was probably for a neon type.

4.3.3.2 Inverter

The Inverter converts a DC input E_C into an AC output that can be transferred, via transformer action, to secondary coils appropriate for the required DC outputs in the 5 V to 250 V range. A

simplified circuit for the Inverter is provided in Fig. 31 (which is a slight modification of Figure 9 in Ref. 16). The transformer is an integral part of the inversion process and its properties set the Inverter's operating frequency.

A single-transformer-saturating-core type of square wave inverter employing a common base connection for the switching transistor was chosen. As a suitable transformer was not commercially-available an in-house version was produced. A Ferox cube type 3B2 core was used in spite of its saturation not being particularly sharp and changing markedly with temperature. In this application tight frequency of operation was not a requirement. The nominal frequency of operation was estimated in Ref 16 p15. The equation for its calculation is:

$$f = \frac{V}{4(N_1 - N_F)B_M A}$$ in mks (metre-kilogram-second) units.

$$f = \frac{V10^8}{4(N_1 - N_F)B_M A}$$ in cgs (centimetre-gram-second) units.

Using the cgs equation and substituting:

$V = 28$
$N_1 - N_F = 100$
$B_M = 3500$ gauss
$A = 1.29$ cm^2

gives $f = 1550$ Hz at 20^{O}C.

At that frequency filtering demand for the rectified outputs from the inverter transformer would be minimal.

4.3.3.3 Regulated DC Power

The four regulators (for +24 V, –24 V, +36 V and +5 V) use similar circuits to transform AC inputs from the Inverter (Fig. 32) to the required regulated outputs. Four-diode bridges with shunt capacitor filters provide the DC inputs to the regulators. A series type regulator circuit using a two-stage amplifier is used for each supply.

+24 V Regulated Output

The complete circuit for the +24 V regulator is shown in Fig. 33 (which is a copy of Figure 14 in Ref. 16). A 6.8 V type Z2A68 Zener diode provides the voltage reference for this regulator. When the collector load resistor of the BCZ10 transistor was connected to the negative side of the unregulated input, poor regulation under conditions of varying input voltage resulted because of the large excursions of collector current and hence of base current to this transistor. Since a –24 V regulated output was required, it was convenient to connect the collector resistor of the BCZ10 to that supply and hence stabilize the collector current with respect to input voltage variations. The 0.022 μF capacitor added between the collector of the BCZ10 and the +24 V rail reduced a significant tendency of the circuit to oscillate by reducing the high frequency loop gain.

The 0.022 μF capacitor value is what was indicated in the Ref. 16 +24 V regulator figure but a value of 0.22 μF was indicated in the Ref. 16 text. During development the required value was determined experimentally and the author does not now know which is correct.

Since changing the value in the text of the current document is easier than changing it in the figure, the value used in the figure has been adopted. The same inconsistency applies for the –24 V regulator.

The following measurements were made on the supply:

Output resistance	0.50 ohm
Change in output voltage as supply voltage changes from 21 V to 30 V at 60 mA current	24 mV
Ripple voltage at 60 mA output current	1.1 mV RMS
Drift over one hour	5 mV

–24 V Regulated Output

A block schema of this regulator is shown in Fig. 34a (which is a copy of Figure 15 in Ref. 16) and the complete circuit is shown in Fig. 34b (which is a copy of Figure 17 in Ref. 16). The voltage reference for this regulator is the +24 V regulator output.

The following measurements were made on this supply:

Output resistance at 28 V unreg. input Output resistance at 21 V unreg. input	0.22 ohm 0.70 ohm
Change in output voltage as supply voltage changes from 21 V to 30 V at 60 mA current	54 mV
Ripple voltage at 60 mA output current	18.5 mV RMS
Drift over one hour	46 mV

+36 V Regulated Output

A block schema of this regulator is shown in Fig. 35a (which is a copy of Figure 18 in Ref. 16) and the complete circuit is shown in Fig. 35b (which is a copy of Figure 19 in Ref. 16). The voltage reference for this regulator is the +24 V regulator output.

The following measurements were made on this supply:

Output resistance	2.3 ohm
Change in output voltage as supply voltage changes from 21 V to 30 V at 30 mA current	54 mV
Ripple voltage at 60 mA output current	3.5 mV RMS
Drift over one hour	75 mV

+5 V Regulated Output

A block schema of this regulator is shown in Fig. 36a (which is a copy of Figure 20 in Ref. 16) and the complete circuit is shown in Fig. 36b (which is a copy of Figure 21 in Ref. 16). The voltage reference for this regulator is the +24 V regulator output.

The following measurements were made on this supply:

Output resistance	0.20 ohm
Change in output voltage as supply voltage changes from 21 V to 30 V at 30 mA current	7 mV
Ripple voltage at 60 mA output current	0.35 mV RMS
Drift over one hour	3 mV

4.3.3.4 Unregulated DC Power

A voltage doubler employing high voltage selenium rectifiers was used to provide the required +250 V unregulated output. The type 36 EHT 13 rectifier will take 2 mA continuous current. To reduce starting currents in the rectifiers to within safe limits the capacitance of the capacitors must not be too large. That requirement was fulfilled using 0.022 µf capacitors. The complete circuit for this supply is provided in Fig. 37 (which is a copy of Figure 13 in Ref. 16).

The following measurements were made on this supply:

DC output voltage for 28 V converter input	275 V
Output resistance	37000 ohm
Ripple voltage at 600 µA output current	2.3V RMS

4.3.4 Provision of AC Output

The Recorder motor was a 400 Hz four-pole three-phase hysteresis type (Smiths HMIZ/2) which ran at synchronous speed. The author was unable to find a specification for this motor. It is assumed it required a nominal 200 VAC between phases which translates as $200/\sqrt{3}$ or 115 V phase to neutral (usually grounded). The power source was E_C which was normally the aircraft's 28 VDC supply but, if the aircraft DC supply failed, the 24 V-nominal emergency battery supply would take over.

An inverter (DC to AC converter) was required to provide the requisite AC power output. Although the motor was a three-phase type, it was possible to run it from a single-phase supply by using a capacitor to produce some phase shift between a pair of phases. Some experiments using square wave drive indicated that the motor could be run from a square wave source. A square wave output at a nominal 160 VAC was the design choice but it was shown experimentally that the motor performed correctly over a wide range in voltage and hence voltage stability was not a prime consideration in the inverter design.

The two-transformer inverter described in Ref. 17 was found to not have the requisite frequency stability for this application although the output transformer for that application was copied for this application. It was found necessary to use a separate oscillator to drive the output stage.

Typical Class B Output Stage

A typical class B push-pull output stage employing a phase-splitting drive transformer was used as shown in Fig. 39 (which is a copy of Figure 5 in Ref. 16). The output transformer was designed for linear operation. As a separate oscillator was to be used in this inverter,

the drive transformer was also designed for linear operation. As will be indicated later the "SUPPLY" was 20 VDC.

400 Hz Square Wave Oscillator

The basic oscillator circuit employed was a relaxation type using a unijunction transistor. The output of the basic oscillator was a series of short duration pulses at 800 Hz frequency. The basic circuit, with components given identification labels to facilitate analysis, is drawn in Fig. 40 (which is a copy of Figure 7 in Ref. 16). Assuming the capacitor C is initially uncharged, then charging will continue until the emitter-base junction of the unijunction transistor becomes forward biased. This voltage (V_P) is given by:

$$V_P = \eta V_{BB} + V_D$$

Where η is the Intrinsic Stand-off Ratio and is constant for a given unijunction transistor over a wide range of temperature and inter-base voltage. V_D is about 0.7 V at 25^{O}C and decreases with temperature at about 3 mV/^{O}C. V_{BB} is the inter-base voltage which is approximately equal to V for R_2 and R_3 small compared with the inter-base resistance.

When the voltage across capacitor C reaches V_P the emitter becomes forward biased, the emitter to base resistance drops rapidly to a very low value, and capacitor C discharges rapidly into the emitter circuit. The circuit returns to the cut-off condition when the emitter voltage has fallen to its minimum value (referred to as the "valley" point) and the process is repeated.

Neglecting the discharging time of capacitor C, since this will be small compared to the charging time, the period of oscillation is given approximately by the time taken for capacitor C to charge to the peak point voltage. If V_D is neglected:

$$V_P \approx \eta V = V\left(1 - e^{-\frac{T}{R_1 C}}\right) \text{ where } T \text{ is the period.}$$

$$T \approx R_1 C \ ln\left(\frac{1}{1-\eta}\right)$$

$$f \approx \frac{1}{\mathrm{R_1 C \ln}\left(\frac{1}{1-\eta}\right)}$$

where f is the frequency of oscillation and is independent of supply voltage.

For the type 2N1671 unijunction transistor used, $\eta \approx 0.5$. For capacitor C the value of capacitance chosen was nominally 0.12 μF. Hence:

$$R_1 = \frac{1}{f \ C \ ln\left(\frac{1}{1-\eta}\right)}$$

$$= \frac{10^6}{800 \times 0.12 \times \ln 2}$$

$$= 15000 \ ohm$$

Actually, about 18000 ohm was needed. A 16000 ohm resistor in series with a 5000 ohm potentiometer for frequency adjustment was used.

Resistor R_2 was used for temperature compensation and the requisite value was based on a formula provided in a reference by J.P. Silvan listed in Ref. 16. A search by the author to find a copy of that reference or an alternative was unsuccessful at the time of writing. Silvan's formula was:

$$R_2 \approx \frac{0.70R_{BB}}{\eta V} + \frac{1-\eta}{\eta} R_3$$

where R_{BB} is the inter-base resistance which was about 7500 ohm for the unijunction transistor used.

For $V \approx 24$ volt and $R_3 \approx 100$ ohm (see below), $R_2 \approx 538$ ohm. Actually, a 470 ohm resistor was used.

A low impedance output, in the form of short duration positive going pulses, was formed across resistor R_3. The value of R_3 was not critical and was made 100 ohm. For improved stability the supply for the basic oscillator was taken from the +24 V regulator.

The oscillator output was coupled to a symmetrically triggered binary. As the binary supply was taken from E_C (+28/24 VDC) a square wave of about 24 V amplitude appeared on each collector. The input for the drive transformer in the output stage was taken between the collectors of each half of the binary, thereby doubling the square wave amplitude in comparison to that appearing at each collector. The complete oscillator circuit is shown in Fig. 41 (which is a copy of Figure 8 in Ref. 16).

Series Regulator and Inverter Output Stage

It was found experimentally that the three-phase recorder hysteresis motor could be run reliably from a square-wave single-phase power source. The final circuit is drawn in Fig. 42 (which is a copy of Figure 6 in Ref. 16). The full load requirement was approximately 20 volt-amp at 0.8 power factor (inductive) for a 400 Hz sinusoidal drive. For square wave output the requisite output was somewhat higher (of the order of 25 volt-amp).

The output transformer was identical to the one described together with a full analysis in Ref. 17. As indicated in that reference the core was a product of English Electric Company (Type Z2371018 consisting of two C-cores made of 0.004 inch strips of silicon steel). The locally added coils comprised a primary consisting of two 180 turn bifilar-wound coils and a secondary of a 1440 turn coil. The power required was far in excess of that available from the regulated DC-output supplies. The E_C (+28/24 VDC) input provided the power source for the inverter. A 20 VDC regulator (Fig. 42) provided a constant input to the 2N1160 power transistors connected to the output transformer primary.

While the 20 V primary input to the output transformer provided a nominal 160 V square wave secondary amplitude (320 V peak to peak), at full load that could drop to about 150 V. It was shown experimentally during laboratory tests that the output transformer secondary voltage could vary over a wide range without compromising the movement of the motor-driven recorder magnetic wire spools. Proper operation of the recorder motor was confirmed in the 23 March.1962 Flight Memory System validation flight.

Part C: Ground System Signal Recovery

5. Ground System

A simplified block schema of the Ground System, as it was set up after the 1962 validation flight, is shown in Fig. 43. During the development of the Ground Station Unit, it was assumed that the input to this unit was the playback signal from the magnetic wire recorder.

The use of the tape recorder in lieu of the wire recorder greatly simplified the recording of the flight results for which multiple passes were required. Copying of the signal recorded on magnetic wire to a magnetic tape recorder (Rola Model 66) was performed by Dr Warren.

There is no written account of how the copying was achieved. It is known that the magnetic wire record-heads were used for both recording and replaying. The airborne recording system described in Sec. 4.1 does not have a simple rewind option but by advancing the wire forward the recording start point would eventually be reached. If this method were used, it would have been necessary to ensure the erase head received zero signal and that the record heads also received zero input signal. Since the magnetic wire recording/replaying heads were the same as that used for the Minifon P55 wire recorder, it is possible that the relevant pair of spools used in the 1962 flight validation test, of short flight duration, could have been replayed on the P55.

The External Equipment items that were connected to the Ground Station Unit output were mainly for use in the analysis of the recorded 1962 flight data.

The Ground System comprised three major sections:

1. Playback Signal Source for the Ground Station Unit
2. Flight Memory Ground Station Unit.
3. Support Equipment for the Ground Station Unit output.

The sections listed above will be considered in the list order.

A block schema of the Ground Station Unit (GSU) is shown in Fig. 44 together with the external input source and the external devices used to display its outputs.

5.1 Playback Signal Source

At the time of the GSU development it was assumed that the signal source would have been the Flight Memory magnetic wire recorder and hence measurements were made by the author on the characteristic of the signal from that source.

The overall frequency response of the Flight Memory wire recording system's record/ playback deck (voltage on playback for constant amplitude record current) was measured and plotted in Ref. 8 (Figure 3). The magnitude of the bias current was indicated as 250 μA DC (should have been indicated as AC and the author will assume it was a peak value). The AC record-current was indicated as 200 μA peak (assumed to be the 100% signal value). The correctly annotated frequency response graph is shown in Fig. 45.

The record/playback head impedance as a function of frequency was plotted in Ref. 8 (Figure 4). There was a labelling error in that figure. The vertical axis marked as KILOHM should have been OHM and likewise the DC resistance should have been 2.2 OHM. From the corrected figure, the record/playback head impedance at 4 KHz would equal 600 ohm. If *L*

represents the record-head inductance and f the frequency, then the record-head impedance would be equal to $2\pi fL$. Using ($2\pi fL$ = 60 ohm at 4 KHz), gives (L = 2.4 mH {milliHenry}) which is a reasonable value for a record-head inductance. The correctly annotated head-impedance graph is shown in Fig. 46.

For a 100% recording current (200 μA peak) at 1000 Hz, the measured playback voltage (Fig. 43) was 2.2 mV peak.

As indicated in Fig. 43, the output of the wire recorder was copied to a tape recorder for ease of handling the cockpit voice and flight data information for the 1962 system validation flight, which required multiple passes. The copying was performed by Dr Warren and the details of how this was achieved is not known to the author. One possibility would have been to remove the relevant two-spool set from the Flight Memory recorder and replay the record using the Minifon P55 Type S Recorder as a replay device. Irrespective of how the copying was done, a simple voltage divider could have been used to set the magnetic tape output to a similar level as that for the Flight Memory recorder.

5.2 Flight Memory Ground Station Unit

The Ground Station Unit comprises four main sub-elements of varying complexity:

1. Pre-Amplifier (to amplify the low-level playback signal).
2. Cockpit Voice Processor
3. Flight Data Processor
4. Power System

The sections listed above will be considered in the list order.

A front-on photograph of the total GSU is shown in Fig. 47. Right and left side photographs of the GSU outside of its enclosure are shown in Fig. 48 and Fig. 49 respectively. At the left-top-rear of the GSU there is an empty rectangular cuboid space. An internal speaker attached to the case wall used some of this space for an internal loudspeaker which allowed the listening of cockpit voice audio. A SPKR output on the GSU front panel (Fig. 47), that was used primarily for use with an external plotter, was also available.

Circuit details and functional support information for all the GSU items except the Flight Data Decoder and Output Generator (Fig. 44) are provided in Ref. 8. Capacitance values in that document are indicated in M or K units which indicate values are in 10^6 or 10^3 picofarad units respectively. Thus, M can be replaced with μF and nK by ($n \times 0.001$ μF). Circuit details and functional support information for the Flight Data Decoder and Output Generator are provided in Ref. 18. Both Ref. 8 and Ref. 18 were written by the author.

5.2.1 Pre-Amplifier

The two-stage Pre-Amplifier (Fig. 50) had negative feedback from the collector of the second stage to the emitter of the first stage, and provided stable gain and a relatively high input impedance. An analysis of the pre-amplifier circuit is given in Ref. 8. From this analysis typical values of voltage gain (53.5), input resistance (243 K) and output resistance (640) were derived, where resistance values are in ohm.

To enable the overall frequency response to be made flatter over the frequency band of interest, provision had been made to switch in a bridge T network to follow the pre-amplifier. That switch is visible on the front panel of the GSU (Fig. 47). The network was designed such that minimum transmission occurred at the frequency corresponding to the peak of the normal response curve (approximately 1300 Hz). As the noise level was increased somewhat in the compensated system, provision had been made to operate the pre-amplifier compensated or flat by means of the selector switch. Details of the bridged T network are given in Fig. 51. For the uncompensated system an attenuator has been added to the output of the pre-amplifier (see Fig. 51) such that the output levels for the respective compensated and uncompensated systems are equal. The responses of the compensated and uncompensated systems are compared in Fig. 52.

5.2.2 Cockpit Voice Processor

The Cockpit Voice Processor comprises three major sections:

1. Cockpit Voice Extractor.
2. Cockpit Voice Power Amplifier and Speaker.
3. Cockpit Voice Voltage Level Indicator.

The sections listed above will be considered in the list order.

5.2.2.1 Cockpit Voice Extractor

The Cockpit Voice Extractor uses an audio band-pass filter to extract the cockpit voice component from the Pre-Amplifier output which includes the frequency multiplexed cockpit voice and flight data.

As the speech filtering requirements for playback are virtually identical to those for the airborne recording. The playback filter has been made the same as that used in the airborne recording unit. That filter was designed by Mr Sear. It comprised a high-pass filter with 400 Hz cut-off frequency and a low-pass filter with 2400 Hz cut-off frequency. A clipper was inserted between the high-pass and low-pass filters for the recording phase. That has been omitted for the playback phase. The band-pass filter circuits and performance are described in Sec. 4.2.2.1.1.2. The high-pass filter circuit is drawn in Fig 12, the low-pass filter circuit in Fig. 13, and the overall frequency response of the band-pass filter in Fig. 14. That response was indicative of a very high-grade band pass filter.

It was noted in Appendix 6 that a regular undefined audio signal (of relatively low volume) could be heard at the ground station recovery stage when no voice signal was present on the recorded audio channel. The flight data comprised sine-wave bursts of 3500 Hz. It was shown that such sine-wave bursts could contain fold-back components that were within the Flight Memory audio pass-band. It was not possible to remove such components at the ground station recovery stage. It was shown that eliminating the problem would have been straight forward once its cause was established. Use of a 3000 Hz high-pass filter for the flight data at the recording stage was suggested as a means of resolving the problem.

5.2.2.2 Cockpit Voice Power Amplifier and Speaker

To raise the level of the cockpit voice signal sufficiently to drive a loudspeaker, a power amplifier is required to follow the filter. Details of the circuit are shown in Fig. 53. That figure

and associated text closely resembles that described for Ref. 8. The output stage of this amplifier is of the single ended push-pull variety with capacitive coupling to the speaker. Phase splitting is provided by a complementary pair of transistors which make up the driver stage. Both driver and output stages are designed for class B operation.

A class A amplifier employing a single transistor precedes the phase splitter. Neither a driver transformer nor an output transformer is required with this circuit. The bias for the various transistors has been derived from the −24V regulated supply whereas the output and driver stages draw their power from the unregulated −32V supply.

Resistors R338, R339, R340 and R341 are chosen such that the output transistors have equal DC collector to emitter voltage drops, or in other words, such that the output point is at approximately 16VDC. In order to reduce cross-over distortion in the class B stages a small amount of forward bias is required. Increasing resistor R342 or adding more diodes between the bases of the complementary pair, Q311 and Q312, will tend to reduce the cross-over distortion. Both DC and AC feedback are provided by R338 and R343. Feedback capacitor C326 removes the tendency of the circuit to oscillate at high frequency. The R337 and C325 combination has a bootstrapping effect which enables higher voltage outputs to be obtained.

The loudspeaker is a type 10-3G of Rola manufacture having a 3.5 ohm voice coil. It has a frequency response which is flat within 30 db from 105 Hz to 6000 Hz According to the manufacturer the speaker will handle 3.5 watt peak. Hence the peak voltage requirement for the speaker is 3.5 volt, a value which is adequately accommodated by this amplifier.

The voltage gain of the amplifier, as drawn in Fig. 53, is defined as the voltage at the speaker terminal divided by the voltage at the R101 volume control wiper. The mid-band voltage gain is 0.5 (2.5 after the 12K input resistor). The −3 db frequency response limits are 40 Hz and 9000 Hz.

5.2.2.3 Cockpit Voice Voltage Level Indicator

For crash investigation purposes it is desirable to be able to relate, chronologically, the motions of the aircraft with any comment or exclamation made by any member of the aircraft flight crew. If the speech level is recorded together with the decoded flight data (in analogue form) on a chart recorder, it is possible using a little care, to associate individual words uttered with the motion of the aircraft at that instant.

Circuit details of the Voltage Level Indicator are provided in Fig. 54. The Indicator's input is connected in parallel with the Cockpit Voice Power Amplifier input which is connected to the Cockpit Voice Extractor output. Potentiometers for positioning the trace on the chart (zero adjustment) and for amplitude setting (attenuator adjustment) were added for specific use with an external Speedomax (l0 mV full-scale) potentiometric recorder. The circuit's Speech/Data switch and the above-mentioned potentiometers are accessible from the mid-section of the GSU's front panel (Fig. 47).

Define the voltage gain of the amplifier as the voltage at the speaker terminal divided by the voltage at the R101 volume control wiper. With that definition, the voltage gain of the amplifier would have been 0.5. The R101 volume control potentiometer was accessible at the top left of the GSU's front panel (Fig. 47).

A Tone adjustment is shown on the top right of the GSU front panel (Fig. 47). That adjustment is not shown on any Cockpit Voice circuit and it is unlikely that its use was ever implemented. The Tone adjustment would have modified the overall frequency response of the cockpit voice channel which might have been regarded as a backward step.

5.2.3 Flight Data Processor

The Flight Data Processor comprises two major sections:

1. Flight Data Extractor.
2. Flight Data System after the Extractor.

The sections listed above will be considered in the list order.

The Flight Data Processor (FDP) is considerably more complex than the Cockpit Voice Processor which basically handles a single input channel. The FDP comprises multiple data channels and multiple output data formats. Details of FDP functions and the circuits developed prior to the 23 March 1962 system validation flight are provided. The flight results are considered in Sec. 5.3.

5.2.3.1 Flight Data Extractor

A filter was required to extract the modulated flight data from the composite speech plus data signal appearing on playback. A basic requirement of the filter was that it provide high rejection of signals within the 400 Hz to 2400 Hz audio band. The pre-recorded flight data signal consisted of a chain of abruptly switched sinusoidal carriers of frequency 3500 Hz. The amplitude envelopes of these bursts were close to perfect rectangles as indicated in Fig. 55. Bandwidth limits for the magnetic wire recording process would have meant that the sharp transitions at the leading and trailing edges of the sine-wave bursts would not have been reproduced on playback. Additional filtering may have occurred on playback

As the frequency spectrum of recovered Flight Data was very broad, it would have been impossible to reproduce it faithfully using a narrow band filter. Since the upper limit of the adjacent speech channel was at 2400 Hz, the filter bandwidth could not have been made too broad. As a practical compromise, a band-pass filter having a bandwidth of 600 Hz centred at 3500 Hz was designed.

The actual filter was an active type using R and C components. By placing a notch network (parallel T) in the feedback loop of a transistor amplifier, a response which peaks at the frequency of the notch results. The degree of selectivity or effective circuit Q depends on impedance levels, transistor current gain and the sharpness of tuning of the notch. To obtain a bandwidth of about 600 Hz and at the same time provide adequate attenuation at 2400 Hz, stagger tuning of two similar stages was employed.

The circuit of the complete filter is drawn in Fig. 56. Tuning of the filter has been achieved using decade capacitance boxes in place of the capacitors in the parallel-T networks. By upsetting the symmetry of the parallel-T network the degree of peaking can be controlled. When the required response is obtained the capacitors may be selected to close tolerance (better than 1%). The frequency response of the filter is drawn in Fig. 57. It is to be noted that the rate of attenuation on the high frequency side of the band pass filter is not as high as on the low frequency side. This has been made deliberately so, as the demands on attenuation for the high

frequency side are not as stringent as for the low frequency side. However, an improvement in signal to noise ratio results by virtue of the attenuation of the high frequencies. The overall gain of the filter at 3500 Hz (output at T5 divided by input at T2: refer to Fig. 57) is 4.8. If the centre band gain is defined as 0 db, then the attenuation at 2400 Hz is about −40 db, which easily met the requirement.

It was shown in Sec. 4.2.2.1.3.1 and Appendix 6 that components of the pre-recorded flight data signal were transferred to the cockpit voice band. Removal of those components via the ground system was not possible.

The author relates (Appendix 8) the rate of rise and decay of the filtered sinusoidal wave-train to that for the unit-step response of a high pass filter having half the bandwidth of that for the band-pass filter. It can be seen from that analysis that, for a given filter configuration, the rate of build-up or decay of the Flight Memory band-pass filter's output is a function of the filter's bandwidth. The frequency response is flat (Fig. 57) in the region of 3500 Hz.

5.2.3.2 Flight Data System After Extractor

The Flight Data System after the Extractor comprises two major sections:

1. Flight Data Decoder.
2. Flight Data Output Generator.

The sections listed above will be considered in the list order.

A block schema of the *Flight Data System after the Extractor* is provided in Fig. 58 together with the external equipment to which the output signals from it are passed.

5.2.3.2.1 Flight Data Decoder

The Flight Data Decoder comprises four major sections:

1. Frequency Doubler.
2. Pulse Duration Replicator.
3. Ramp Generator.
4. Synchronised Oscillator.

The second item is referred to in Fig. 58 as the *Pulse Duration Replicator* which is a better indicator of its function than the equivalent *Gate Forming Circuit* that was used in Ref.18. The term *Gate* is used in the *Output Generator* (Fig. 58) where that is more appropriate.

The sections listed above will be considered in the list order.

5.2.3.2.1.1 Frequency Doubler

The signal entry item (see Fig. 58) for the decoder is, for convenience, referred to as the "Frequency Doubler". Such a name implies a rather simple circuit as, for instance, a full wave rectifier. While it is true that a full wave rectifier is used as the basic frequency doubler (changing the 3500 Hz signal into a 7000 Hz signal) the combined input circuit is considerably more complex. Although it is used for other purposes, the frequency-doubled output is generated mainly because it enables half cycle resolution of the modulated flight data input signal to be realized.

The block schema of Fig. 58 reveals, in general form, the composition of the frequency doubler. Essentially the input data signal, which is the output from the Extractor (Band-Pass Filter), is first amplified, then passed through a full wave rectifier which doubles the frequency. To provide a suitable signal for the "external frequency standard" terminals of the external Electronic Counter (to be referred as just "counter" in this section) and also for the Pulse Duration Replicator a Schmitt trigger circuit is used. The input to the Schmitt trigger circuit follows the amplitude pattern depicted in Appendix 8.5 (Fig. A11). For a constant 100% amplitude input signal, the number of pulses formed by the Schmitt circuit would be reasonably constant for a given sample, provided the trigger level of the Schmitt circuit is kept well clear of the input signal low or high extremes. Ideally, the number of cycles in a given full-wave burst should equal the number at the time of recording. Because the shape of the trailing edge of the burst is an inverse of that for the leading edge (Appendix Fig. A11) a half cycle difference is likely. SYNC and ZERO reference channels would allow differences to be managed without loss of accuracy. As the leading edge of the first pulse from the Schmitt circuit also defines the leading edge of the gate signal fed to the counter, it is essential that for consistent counting the Schmitt circuit triggers at the same relative level on each sample of the modulated flight data.

Amplitude variations inherent in the record/replay systems lead to some uncertainty in the count registered by the counter. If the trigger level is set to, say, 40% of nominal amplitude, then a ±10% amplitude variation, occurring just when the Schmitt circuit is about to trigger, will cause a ±1 count variation (actually 0.5 % since half cycles are being counted). It is to be noted that the data filter has been designed such that 5 complete cycles (10 half cycles) lapse before the modulated data input signal builds up to full amplitude. Similar count uncertainties result by virtue of amplitude variations occurring on the trailing edge of the modulated data pulse.

Amplitude variations inherent in the input signal can be divided broadly into two types: relatively rapid fluctuations and relatively slow variations.

In the "rapid fluctuation" group there is a ±10% amplitude jitter produced partly by short term variations in recorder overall gain (which may be caused by roll of the magnetic recording wire, fluctuations in contact pressure between the wire and the head on either record or playback or the presence of dust particles on the head or the wire) and, partly because of the presence of a random noise signal falling within the band of the flight data filter. Also included in the rapid fluctuations of amplitude are signal drop-outs, arbitrarily defined here as amplitude reductions greater than 50% of normal amplitude. Measurements made with a continuous 3500 Hz note revealed that, using a Minfon P55 as a replay device, about one drop-out every 3.3 seconds could be expected. Complete signal drop-outs having a duration of up to 30 cycles of the 3500 Hz signal occur occasionally. Signal dropouts are produced if the wire separates from the head momentarily, either during record or playback. Apart from designing the decoder to minimise the tendency of the system to temporarily lose synchronism when drop-outs occur, nothing else was done regarding rapid amplitude variations. The effect of a slowly varying type of amplitude change can be more readily eliminated. Long term variations in amplitude may be caused by any long-term drift in the overall gain from record to playback. For instance, as the rotational speed of the wire spool and not the linear speed of the wire itself is governed, the signal amplitude will vary as a spool is unreeled.

To eliminate the effect on the half-cycle output count of a long-term amplitude variation, an automatic gain control (AGC) circuit, as depicted in the Fig. 59 block schema, has been incorporated in such a way as to maintain a close to constant amplitude output from the basic frequency doubler circuit. The AGC is a complex circuit that can be most readily understood by reference to Fig. 59. The *Amplitude Reference* shown in that figure controls the closed loop low frequency gain. The operation of the complete Frequency Doubler circuit, including the AGC element, may be studied with reference to the circuit of Fig. 60. GSU front panel switch S107 allows AGC to be switched *on* or *off*. When *off* a fixed gain will apply.

At various circuit points in Fig. 60 marked with a circle containing an identification number, the waveforms at those points have been drawn in Fig. 61 and will be referred to in the text. Regulated supply rails of +24 volt and −24 volt are employed. Circuit details and performance figures on these supplies will be provided in Sec. 5.2.4.

Circuit operation for the AGC switched *on* will now be examined.

Transistor Q502 and associated circuits constitute a gain controlled common emitter amplifier. As the base of Q502 is virtually fed from a voltage signal source, the stage gain will vary inversely as the input resistance of this transistor. Now the intrinsic emitter resistance r_E varies as the DC emitter current I_E according to the relation:

$$r_E = \frac{K}{I_E}$$

$$K = \frac{kT}{q}$$

$$r_E = \frac{kT}{qI_E}$$

where k = Boltzmann constant (1.38 x 10^{-23} joule/°K)

T = Absolute temperature (°K) noting (°K = °C + 273)

q = Electron charge (1.60 x 10^{-19} coulomb)

Hence $r_E\ (ohm) \approx \frac{26}{I_E\ (mA)}$ $(at\ 27^oC)$.

Referring to Fig. 62(b), which is a small signal equivalent circuit for the gain-controlled amplifier of Fig. 62(a), it follows that voltage gain Av is given by:

$$Av = \left|\frac{e_0}{e_1}\right| \approx \frac{\beta|Z_L|}{r_E} = \frac{\beta|Z_L|I_E}{26} \quad (at\ 27^oC)$$

where β is the current gain for transistor Q502.

Note that Z_L is the effective impedance seen at the collector of Q502. It is the combined load made up of collector-connected resistor R510, capacitor C507, resistor R512, resistor R513 and input resistance of Q503. Assuming the input resistance of Q503 is very low, Z_L can be considered to be close to the impedance of R510 and C507 connected in parallel. The reactance of C at 3500 Hz is equal to 4.55 K. A detailed calculation gives $|Z_L|$ equal to 3.54 K.

Now I_E is controlled by AGC control voltage V_2 according to the relation (refer to Fig. 62(a)):

$$I_E = \frac{R_1 V_2 - R_2 V_1}{R_E (R_1 + R_2)}$$

In the derivation of this expression the emitter base voltage drop of Q502 has been neglected and it has been assumed that the base current is negligible compared with the current in the resistance divider chain.

Substituting R_1 = 180K, R_2 = 120K, R_E =2.2K and V_1 = 24V, we obtain:

$$I_E = 0.27\, V_2 - 4.36\, mA$$

$$\frac{\partial I_E}{\partial V_2} = 0.27\, mA/volt$$

The Q2-amflifier stage had been designed for a nominal DC emitter current I_E of approximately 0.5 mA. Q2 is a Germanium transistor with a regular base to emitter voltage drop of about 0.3 V. In 1961 Germanium transistors were in more common use than the Silicon type. A recalculation of I_E for the AGC switched off and using the R509, R515 and R516 bias network yielded a value of 0.41 mA. That approximates the design value which was probably set up experimentally. The design value of 0.5 mA will be used below.

Fractional change in gain g_c per volt change in AGC control voltage is given by g_c as follows:

$$g_c = \frac{1}{Av} \frac{\partial A_v}{\partial V_2}$$

$$= \frac{26}{\beta |Z_L| I_E} \left(\frac{\partial A_v}{\partial I_E} \right) \left(\frac{\partial I_E}{\partial V_2} \right)$$

$$= \frac{26}{3.54\beta\, I_E} \times \frac{3.54\beta}{26} \times 0.27$$

$$= \frac{0.27}{0.5}\ per\ volt$$

= 0.54 fractional change in A_v per volt change in V_2.

Hence a 1.0V increase in the AGC control voltage will approximately halve the gain of the first amplifying stage. As indicated above the corresponding change in I_E will be 0.27 mA.

Additional amplification is performed via Q503, whilst L601 and associated diodes constitute a full wave rectifier. Q601 acts simply as an emitter follower. The negative-going rectified waveform appearing on the emitter of Q601 is drawn in Fig. 61 waveform No. 2. It has an envelope pattern identical to the input signal amplitude pattern which can be observed in Fig.61 waveform No. 1.

Peak amplitude sampling of the output of Q601 is performed via diode D501 and the associated filter circuit. The filter has a charge time constant of approximately 0.5 second and a discharge time constant of approximately one second. Hence a DC voltage will be formed at the base of Q506 which follows the peaks of the rectified data signal. Transient peaks are ignored by the filter because of the relatively long charging time.

Emitter follower Q506 acts as an impedance buffer for the amplitude sampling side of the DC differential amplifier formed by Q504, Q505 and associated circuit. Potentiometer R102 (Gain 2 adjustment on the front panel of the GSU) sets up a reference DC voltage, typically about −5 V on the other side of the differential amplifier. If a difference voltage exists between the signal amplitude sampling side and the reference side of the differential amplifier, a change in output voltage will appear on the collector of Q505. This voltage is the AGC control voltage and is phased such that the gain of Q502 will be changed so as to make the output amplitude very nearly equal to the reference level set by R102. With this feedback-gain-controlled system a 300% change in input level results in a 7.5% change in rectified output level.

Switch S107 (located on the front panel of the GSU) enables the equipment to be operated with the AGC control "on" or "off." As the AGC circuit takes some seconds to stabilise, it is sometimes inconvenient to operate in this mode when an immediate response is required. Normally R103 (Gain 1 adjustment on the front panel of the GSU) is adjusted, with the AGC in the "off" position, to give the appropriate output level. If the AGC circuit is then switched in, the amplitude level will be maintained in spite of any drifts which may occur in the input signal amplitude.

The amplitude stabilised signal appearing on the emitter of Q601 is taken to the Schmitt trigger circuit made up of Q602, Q603 and associated components. Potentiometer R604 enables the triggering level to be varied. Typically, a triggering level of 2 V (40% of input amplitude) is used as illustrated in Fig. 61 waveform No 3. A chain of square pulses appears at the output of the Schmitt trigger circuit as illustrated in Fig. 61 waveform No. 4. The output of the Schmitt trigger circuit is coupled via capacitor C602 to the Counter External Frequency terminals.

5.2.3.2.1.2 Pulse Duration Replicator

Basically, the function of the Pulse Duration Replicator is to produce rectangular pulses which replicate, as close as possible, the PDM (Pulse Duration Modulator) wave-train (Fig. 55) which was converted to a sine-wave burst wave-train prior to being passed to the airborne system magnetic wire recorder. The duration of each sine-wave burst is a measure of the magnitude of the recording signals (transducers Ch 1 to Ch. 6, Zero-reference Ch 7 and Marker Ch. 8).

The Pulse Duration Replicator produces rectangular pulses which follow the envelope pattern of the batches of pulses appearing at the output of the Schmitt trigger circuit. Such pulses closely match those referred to above for the recording system. The details of the formation of an individual rectangular pulse are described below.

Pulses from the Schmitt circuit pass through diode D608 (see Fig. 63) and charge capacitor C603. Since the output pulses from the Schmitt circuit are effectively "off" pulses, the charging time constant of C603 will be the product of the Schmitt load resistance R607 (10K see Fig. 60) and charging capacitance C603 (1.0 K). Hence the charging time constant will be 10 μs (compare with pulse repetition period of 143 μs). It follows that the charging time is small compared with the Schmitt pulse repetition period.

In Fig. 64 waveform No. 5, the effect of filtering the output of the Schmitt trigger circuit can be observed. Normally (no pulse input), Q604 is held off by reverse bias via R609. When the voltage at the C603-R603 junction reaches approximately −11V, the base of Q604 will become forward biased and this transistor will be switched on. Negative pulses arriving via D603 will charge C603 to approximately the negative supply voltage (−24V) via R607 (Fig. 60). When

the Schmitt circuit output reverts to the "on" state between pulses, D603 will become reverse biased and C603 will discharge towards zero volt with time constant of approximately 150 μs {C603 (1K) multiplied by R608 (150K)}. Typically, C603 may discharge to about $-17V$ before the next pulse arrives (see waveform No. 5 in Fig. 62). The magnitude of this voltage will depend on the triggering level set by the Schmitt trigger circuit, becoming higher in magnitude as the trigger level is reduced.

Subsequent to the arrival of the final pulse, C603 will discharge towards 0V with time constant 150 μs until the switching level of -11 volt for Q604 is reached. At this voltage, Q604 will switch off and the impedance as seen at the base will be high. From this point C603 will charge towards +24V with a time constant of approximately 540 μs {(R608 + R609) x C603}. When approximately $-2V$ across C603 is reached, the voltage will become clamped to the voltage output from the Schmitt trigger circuit via diode D603.

Waveform 6 of Fig. 62 illustrates the rectangular pulse appearing at the output of the Pulse Duration Replicator. The leading edge of this waveform is virtually coincident with the leading edge of the first pulse from the Schmitt circuit whereas the trailing edge of this waveform lags the trailing edge of the final pulse from the Schmitt circuit by approximately 120 μs, which is slightly less than a half cycle period of the 3500 Hz signal. Because of loading due to the Ramp Generator Circuit the "off" level is $-13V$ approximately.

A separate gate signal (to be indicated later) is used when output to an Electronic Counter (digital format) is involved. In that case 0.5% of full-scale accuracy would be maintained. The replicator gate signal examined in this section is used only for analogue voltage output for which lower accuracy is tolerable

5.2.3.2.1.3 Ramp Generator

Basically, the function of the Ramp Generator circuit is to convert the pulse width modulated signal from the Pulse Duration Replicator into a form of proportional pulse height signal. For the digital system, the signal produced by the ramp generator is used in conjunction with a voltage comparator circuit to provide a synchronising pulse each time the marker pulse arrives. As such, the demand on linearity (in respect of the relationship between pulse height and pulse width) is not very stringent for the digital system. However, for the analogue system any non-linearity in the ramp produces a non-linearity in the analogue signal. Hence linearity of the ramp is of prime importance.

The complete circuit of the ramp generator is drawn in Fig. 65. If capacitors C702 and C703 are replaced by a single capacitor, and resistor R705 plus diodes D702 and D703 are removed, a bootstrap sweep circuit similar to the one used in the Pulse Duration Modulator for the airborne system (Sec. 4.2.2.1.2.4) takes form. That modulator circuit was based on a similar circuit described by Williams (Ref. 9).

The input to the ramp generator is the rectangular T7 output from the Pulse Duration Replicator. An output at T23 is a slightly attenuated version of the input gate signal at T7 and has no influence on the operation of the ramp generator under examination here. The output at T23 is passed to the Analogue Converter (part of the Output Generator to be examined later) and is used only when Auto-Calibration mode is selected.

A simplified circuit of the ramp generator is drawn in Fig. 66(a). Transistor Q701 acts merely as a switch gated by the output from Pulse Duration Replicator. For simplicity, the transistor switch in Fig. 64(a) has been replaced by an ideal switch S. In the periods between pulses, the output of the Pulse Duration Replicator is sufficiently negative to ensure that Q701 is on (switch S closed). When Q701 is on, bootstrap capacitor C701 charges via diode D701 to practically the full supply voltage. When a pulse appears at the output of the Pulse Duration Replicator Q701 switches off and bootstrap capacitor C701 begins to discharge via resistor R, capacitor C, the –24V supply, the collector load resistor of Q702, and finally transistor Q702. Since the emitter base voltage of Q702 remains practically constant as C charges, and if it is assumed that the capacitance of C701 is so high that the voltage change across it is negligible during the period for which S is off, a constant current of about $\frac{V}{R}$ will flow into capacitor C. Hence the voltage across C will change linearly with time. When S switches back on again, capacitor C will rapidly discharge to practically 0V.

The actual circuit employed is a slight but significant modification to the one described above. By suitably selecting a resistor in this circuit, compensation for small departures from linearity in the ramp may be made. Moreover, by using "over compensation", non-linearity in the overall voltage analogue may be minimised.

The circuit modification was developed by the author to provide a ramp with a slight bend in the opposite sense to the droop that can occur in conventional ramp generators. The author is unaware of anybody who had used such a technique prior to his development or has used it subsequent to his development.

Usually, departures from ramp linearity follow the form depicted in Fig. 67. The extent of the departure from linearity increases with time. Expressed analytically

$$\frac{\Delta v}{v} = kt$$

where v is the ramp voltage, t is time and k is the ramp slope

If capacitor C is split to form C_1 and C_2 and a resistor Rc is connected as shown in Fig. 66(b) the following equations apply after making normal simplifying assumptions (base to emitter voltage and base current of Q702 are near enough to zero).

$$i_1 = \frac{V}{R}$$

$$i_2 = \frac{V}{R} + \frac{v_{C_1}}{R_C}$$

where the voltage and current symbols are used for the circuit as indicated in Fig. 66(b).

If it is assumed that the capacitors are initially uncharged then the following equations apply.

$$v_{C_1} = \frac{1}{C_1}\int_0^t i_1 \, dt$$

$$= \frac{1}{C_1}\int_0^t \frac{V}{R} \, dt$$

$$= \frac{Vt}{RC_1}$$

$$v_{C_2} = \frac{1}{C_2}\int_0^t (i_1 + i_2)\, dt$$

$$= \int_0^t \left(\frac{V}{R} + \frac{Vt}{RR_C C_2}\right) dt$$

$$= \frac{Vt}{RC_2} + \frac{Vt^2}{2RR_C C_1 C_2}$$

$$v = v_{C_1} + v_{C_2}$$

$$= Vt\left(\frac{1}{RC_1} + \frac{1}{RC_2} + \frac{1}{2RR_C C_1 C_2}\right)$$

Putting $C_1 = C_2 = 2C$ we obtain

$$v = \frac{Vt}{RC}\left(1 + \frac{t}{8R_C C}\right)$$

$$v = \frac{Vt}{RC} + \frac{Vt^2}{8RR_C VC^2}$$

For ($R_C = \infty$) only the normal linear term remains. The expression above implies an left ward bend in the ideal ramp and can be used to compensate for the tendency of the ramp to droop. The correction is parabolic {having zero value at (t = 0) and increases as t increases}.

As the basic ramp was linear to approximately 0.5%, not much compensation was required to linearize the ramp, but to linearize the voltage analogue "over compensation" may be employed.

Assume that the ramp requires x% correction at t = T

$$\frac{\Delta v}{v} = \frac{T}{8R_C C} = \frac{x}{100}$$

$$R_C = \frac{12.5\, T}{xC}$$

For x = 0.5 at T = 34 msec, and for (C = 410K picofarad) then ($R_C = 2.08M$).

It had been assumed that both capacitors Cx and C2 were initially discharged. To ensure that this was the case, it was necessary to add diodes D702 and D703. In the absence of D703, a positive voltage may develop across C703 and, alternatively, in the absence of D702, a negative voltage may be developed.

Ramp voltages appear at both base and emitter of Q702. In the circuit employed (see Fig. 65), the emitter waveform has been used and has been passed to emitter follower transistor Q703. The emitter follower prevents loading on the ramp generator circuit. In Fig. 68 waveform No. 6 has been redrawn on a different time scale to present a typical data sample of all channels. Negative going ramp waveforms, produced when the output of the Pulse Duration Replicator

gated Q701 off, have been drawn in waveform No. 7 of Fig. 66. Note that the marker channel produced a ramp height greater than that from any other channel.

Switch S104 is a double-pole double-throw switch with A and B added to indicate the separate poles. For the above analysis, it has been assumed that switch S104A is in the –24V position. It will be shown later that, in the "AUTO CAL" position (see GSU front panel: Fig. 47), it is possible to perform automatic calibration.

Potentiometer R706 in Fig. 65 enabled the ramp slope to be adjusted over a wide range. A ramp slope of approximately 0.29 V per millisecond was used.

5.2.3.2.1.4 Synchronised Oscillator

If a signal dropout of sufficient duration occurs during replay of the flight data signal, an additional switching pulse will be generated by the Pulse Duration Replicator (PDR). Similarly, if a random burst of signal appears during an "off" period between data samples, an additional pulse may be formed by the PDR. In order that the binary counter (described later) be set to switch in proper synchronism, it is imperative that the counter receive trigger pulses corresponding only to the commencement of data pulses (or, in other words, the leading edges of pulses formed at the output of the PDR - see waveform No. 6 in Fig. 68). Any additional pulses, formed for the reasons described above, would cause the count to advance in the binary chain if the output from the PDR were used as the counter trigger source. For example, if a dropout were to occur during the data sample for channel 1, all succeeding samples up to the marker channel (when a counter synchronising pulse is produced) would be gated to the wrong channel.

To virtually eliminate the tendency of the system to temporarily lose synchronism because of the presence of signal dropouts, an astable multivibrator has been incorporated. Ref. 19 provides details on the operating principle of the astable multivibrator. The un-triggered multivibrator free runs at a frequency slightly less than the incoming sampled data rate (24 Hz nominally). In the triggered mode of operation, the multivibrator frequency becomes locked to the incoming sampling rate by way of trigger pulses derived from the output of the PDR. By making the individual "on" and "off" periods of the free running multivibrator markedly different, an oscillator can be made which is insensitive to trigger pulses except in the region near the start of a data sample. In this way, most of the unwanted pulses formed because of dropouts or noise pulses do not upset the counter synchronism.

The complete circuit details of the triggered astable multivibrator circuit are presented in Fig. 69. As indicated in Ref. 19, transistor Q605 alternates between being in the "on" and "off" states while the reverse states apply for Q606. For the purposes of analysis, a simplified circuit, with triggering components omitted, has been drawn in Fig. 70(a). For ease of analysis the zero-reference voltage has been taken as the common emitter point in this circuit. The "on" and "off" times of the output waveform will be proportional to R_2C_2 and R_1C_1 respectively. When the transistors revert to the "off" condition, the collectors will not immediately switch to the collector load resistor supply rail, but will rise towards this voltage with recovery time constant R_LC_1 or R_LC_2. For unsymmetrical period operation it is essential to keep the recovery time constant R_LC_2 (in this case the longest) low. The problem arises because the capacitor which affects the recovery time of the short period "off" pulse in the oscillator output {see Fig. 70(c)} is the one associated with the timing of the long period "on" pulse in the oscillator

output. In order to minimise the recovery times, R_1 and R_2 are returned to a voltage more negative than the collector supply voltage. In this way the values of R_1 and R_2 may be increased, and hence C_1 and C_2 may be reduced to provide the requisite R_1C_1 and R_2C_2 time constants. By reducing the values of C_1 and C_2, the recovery times may be kept low. Note that R_1 and R_2 must be low enough to provide sufficient current to saturate the transistors in the "on" condition.

A simple analysis of the circuit of Fig. 70(a) enables the period of the free running oscillator to be determined. With Q605 "off" and Q606 "on" C_1 will charge to the collector supply rail voltage. When Q605 is switched on, C_1 will have an initial voltage V_{CC} across its terminals and will begin to discharge with time constant R_1C_1 as illustrated in Fig. 70(b). Referring to this figure we may write:

$$i = \frac{2V_{CC} + v}{R_1}$$

$$v = iR_1 - 2V_{CC}$$

$$v = V_{CC} - \frac{1}{C_1}\int_0^t i\,dt$$

(Note that V_{CC} is the voltage corresponding to the initial charge on C_1).

From the above two equations:

$$V_{CC} - \frac{1}{C_1}\int_0^t i\,dt = iR_1 - 2V_{CC}$$

$$\frac{1}{C_1}\int_0^t i\,dt + iR_1 = 3V_{CC}$$

Differentiating we obtain

$$\frac{1}{C_1} + R_1\frac{di}{dt} = 0$$

$$\frac{di}{dt} = -\frac{1}{R_1C_1}$$

Hence $i = i_0\, e^{-\frac{t}{R_1C_1}}$ $\quad where\ (i = i_0)\ at\ (t = 0)$

$$i_0 = \frac{3V_{CC}}{R_1}$$

$$i = \frac{3V_{CC}}{R_1}\, e^{-\frac{t}{R_1C_1}}$$

$$v = V_{CC}\left(3e^{-\frac{t}{R_1C_1}} - 2\right)$$

Now, when v reaches zero potential approximately, Q606 will switch "on" and Q605 will switch "off". Let ($t = T_1$) when ($v = 0$).

$$Then\ T_1 = (R_1C_1)\ln 1.5$$

$$T_2 = (R_2C_2)\ln 1.5$$

If T_F is defined as the free running period, then

$$T_F = T_1 + T_2$$
$$= (R_1C_1 + R_2C_2) \ln 1.5$$

Further, define *T* as the nominal period of the data samples ($\frac{1}{24}$ second).

Due to imperfections in the record/replay system, *T* will not be absolutely constant but will vary due to recorder wow, pulse width chatter (due to amplitude jitter as outlined in Sec. 5.2.3.2.1.1), and any drifts in the sampling rate of the oscillator in the recording unit. If the wire replay and recording speeds differ, an apparent change in sampling rate will result. The synchronised oscillator has been designed such that the absence of one trigger pulse (as may occur if a dropout occurs at the start of a sample) in a train of trigger pulses will not desynchronise the system. As the probability that dropouts of sufficiently long duration will occur at the start of two consecutive pulses is extremely small, de-synchronisation due to this cause will be a rarity.

Let ± *wT* be the variation in the nominal period *T* due to various causes referred to above. Let that part of *T*, for which the oscillator will respond to start triggers, be denoted by τ {see Fig. 70(c)}. For the system to remain in synchronism with one of a chain of trigger pulses missing (taking into account the maximum deviation in sampling rate), the following equation applies

$$2T_F - 2T(1-w) = \tau$$

Put $T_F = T(1+w)$, the maximum free running period for the system to run synchronously (taking into account the variations in *T*).

$$Hence\ \tau = 4wT$$

Allowing for ±3% wow (record/replay system speed variations), ±2% period change due to amplitude chatter, and ±1 % to cover drift, then it would be conservative to put w = 0.06.

Now *T* = $\frac{1}{24}$sec = 41.7 msec.

$$T_F = 41.7(1+0.06)\ msec = 44.2\ msec$$

$$\tau = 4 \times 0.06 \times 41.7\ msec = 10.0\ msec$$

It was found experimentally that ($\tau \approx 0.7\ T_1$).

Hence T_1 (free running) should be set to 14 msec. C605 has been selected to obtain this value of T_1.

By adjusting R614 (effectively adjusting R_2), T_2 may be varied to make T_F equal to 44.2 $msec$.

Positive going start trigger pulses, derived from the PDR, are diode-gated to the base of Q605 to provide oscillator synchronisation. In Fig. 68 (waveform No. 9) the oscillator output waveform has been drawn. Note that the "off" going edges of this waveform are somewhat rounded due to the finite recovery time. For this waveform the recovery time constant is ($R_LC_2 = R616 \times C06 = 1.8\ msec$).

5.2.3.2.2 Flight Data Output Generator

The Flight Data Output Generator comprises five sections:

1. Voltage Comparator.

2. Binary Counter.
3. Channel Selector and Digital Presentation of Data.
4. Analogue Output Producer and External Presentation of Data.
5. Possible Simple Extension of the Flight Data System.

Item 3 provides a single channel output to an external Electronic Counter which provides a digital output presentation. Item 4 provides a single analogue output for use with an external Chart Recorder.

The sections listed above will be considered in the list order.

5.2.3.2.2.1 Voltage Comparator

The function of the voltage comparator is to provide a synchronising pulse every time a marker pulse arrives. Operation of the comparator circuit may be examined with reference to the circuit diagram of Fig. 71. As the comparator presents a relatively low impedance when triggering occurs, emitter follower Q704 is used to prevent any loading on the ramp input. Loading of the ramp circuit, on triggering of the comparator, is of no consequence in the digital system but it may produce marked non-linearity in the analogue output from the marker channel. Under normal conditions the emitter-base junction of Q705 is reverse biased and only leakage currents flow. The emitter of Q705 follows the negative going ramp voltages of waveform No. 7 in Fig. 68. Prior to triggering, the base of Q705 is held at some negative voltage set by R711. If the magnitude of the negative ramp voltage exceeds the magnitude of the negative voltage on the base of Q705, this transistor will conduct.

For synchronisation purposes, only one pulse each time the marker pulse arrives is required. Hence the triggering level is set between the magnitude of 100% signal ramp and the marker ramp, as illustrated in waveform No. 7 of Fig. 68. With Q705 switched off, Q706 conducts slightly such that an output of approximately +5V appears at T9. When Q705 conducts, Q706 is driven into saturation such that approximately +21V appears at T9. Resistor R713 and capacitor C704 provide positive feedback to the base of Q705 to increase the switching speed. A short duration synchronising pulse, as illustrated in waveform No. 8 of Fig. 68, appears at T9 just before the end of each marker pulse.

5.2.3.2.2.2 Binary Counter

Three symmetrically triggered bistable multivibrators have been cascade-connected, as shown in the circuit of Fig. 72, to form a three-bit (count-by-8) binary counter. Positive trigger pulses derived from the output of the synchronised oscillator are diode gated into the first binary. Collector triggering is employed in what is a fairly conventional binary counter.

To allow coupling capacitors C608, C611 and C614 to discharge between trigger pulses, resistors R620, R627 and R634, respectively, have been added.

Under normal conditions, the “off” transistors are reverse biased from either the +24V rail via R619, R626 and R633, or from the comparator output (which is nominally +5V) via R621, R628 and R635. When a synchronising pulse is generated by the voltage comparator circuit, the voltage at T9 (see Fig. 71) jumps from a nominal +5V to approximately +21V. The latter voltage is high enough to ensure that transistors Q608, Q610 and Q612 are switched off, if they happen to be in the “on” state when the synchronising pulse arrives. Hence the synchronising

pulse serves to set the counter in a given state (or check that it is in a given state) once every complete cycle of eight data samples.

In Fig. 73 the various collector waveforms of the binary counter chain have been drawn. The waveforms are shown in relation to the "start" trigger pulses derived from the output of the synchronised oscillator and also the synchronising pulse generated during the sample time of the marker channel (Channel 8). As there is a total of 8 channels and a divide-by-8 circuit is used, the counter should remain in synchronism (after having been initially synchronised) even in the absence of synchronising pulses. If a signal drop-out occurs during a marker pulse, the ramp output from the ramp generator circuit will be switched back to zero at the time the drop-out arrives and will start from zero again when the drop-out passes. Hence sufficient voltage level will not be reached in the ramp generator output to trigger the voltage comparator, and hence a synchronising pulse will not be generated. For the reasons mentioned above, the absence of the synchronising pulse will not de-synchronise the system. However, should the binary circuit, for any reason, lose synchronism (such as, for example, if the counter is switched to the count 5 state when the channel 4 data sample arrives) the following synchronising pulse, generated when the marker pulse arrives, will restore the synchronism.

5.2.3.2.2.3 Channel Selector and Digital Presentation of Data

When a binary counter, which switches in synchronism with the incoming data samples, has been designed, it is a simple matter to add a diode "AND" gate which will produce a gate signal associated with any desired channel. If only one channel at a time is to be decoded, a 3-diode "AND" circuit connected to the appropriate binary outputs by means of a selector switch may be conveniently used as the channel selector. A simplified block schema of the Channel Selector is drawn in Fig. 74. The "AND" gate output from the Channel Selector was passed to "Time Interval" terminals and the output of the Frequency Doubler circuit to the "External Frequency Standard" terminals of the external Hewlett Packard Type 522B Electronic Counter. In effect, the external Counter would have counted the number of Frequency Doubler output cycles that occurred while the "AND" gate output was in the "1" state.

The Binary Counter (Sec 5.2.3.2.2.2**)** has six outputs corresponding to terminals T11 to T16 as shown in Fig. 72. A more compact designation H to $\bar{L}$ is indicated in Figs. 58 and 74 and reproduced in the following table.

Ch	T11	T13	T15		T12	T14	T16
	H	M	L		$\bar{H}$	$\bar{M}$	$\bar{L}$
1	0	0	0		1	1	1
2	0	0	1		1	1	0
3	0	1	0		1	0	1
4		1	1		1	0	0
5	1	0	0		0	1	1
6	1	0	1		0	1	0
7	1	1	0		0	0	1
8	1	1	1		0	0	0

With the above six outputs, a 3-input AND gate with all inputs in a unique 1-state can be produced for each of the 1 to 8 channels.

Complete circuit details of the channel selector are presented in Fig. 75 with the switch chosen for the Ch 5 position example for that Figure. The 8-position channel selector switch is mounted on the front panel of the GSU (Fig. 47). Each binary output (T11 to T16) has an "on" level of approximately 0V and an "off" level of approximately –21V. The 3-deck channel selector switch S103 connects T11, T13 and T16 to the 3-diode "AND" gate in the channel 5 position. If one or more of these outputs is at 0V, the output at T17 will also be at 0V (approximately. However, if (and only if) all three outputs are at the "off" potential (–21 V), diodes D704, D705 and D706 will be reverse biased, and the voltage at T17 will be at –16V approximately (taking into account loading effects due to voltage analogue circuit to be discussed later). Note that for the diodes to become reverse biased the potential at T18 must be lower in magnitude than the "off" potential from the binary outputs. For this reason, a Zener diode D707 (4.7V nominal) has been added as shown in Fig. 75. With the channel selector switch in the No. 5 position a negative going gate signal as revealed in waveform No. 16 of Fig. 73 is generated between the start of the channel 5 data sample and the start of the channel 6 data sample. A similar gate signal is generated about the appropriate data sample, if the channel selector switch is in any other position.

For a hard-copy record of the chosen channel's count value over time, the Hewlett Packard Type 522B Electronic Counter was coupled to the Hewlett Packard Type 562A Digital Recorder which was capable of typing the required three-digit number three times per second (actually the 562A is capable of providing 11 columns 5 times per second). In this way consecutive readings appeared in rows in the longitudinal direction of the paper tape.

Although the provision of simultaneous outputs for multiple channels would have been simple to achieve (by using a 3-input AND gate circuit for each additional channel), a separate external Electronic Counter would have been required for each additional channel. Therefore, that option was not considered to be viable.

If simultaneous digital presentation of multiple channel information had been desired, the single diode "AND" circuit of Fig. 72 could have been replaced by a diode matrix. As multiple channel presentation required the use of multiple counters, the digital presentation system was confined to a "single channel at a time" presentation.

5.2.3.2.2.4 Analogue Output Generator and External Presentation of Data

This Section comprises five sub-elements:

a. Preview
b. Simple Analogue Output Voltage Generator
c. Practical Analogue Output Voltage Generator
d. Automatic Zeroing
e. Automatic Calibration

These items will be examined in the above order.

Preview

Although the digital method of presentation of the flight data provides optimum accuracy (±1 % °full scale), it is not quite as convenient for observing general variations of a parameter throughout a flight as a continuous graphical recording method. For this reason, it was

considered essential to develop an analogue system of presentation of the demodulated flight data. Numerous methods of producing a suitable analogue signal could have been be used.

In the system which was adopted, the *Ramp Generator* (described in Sec. 5.2.3.2.1.3) produced a ramp voltage the peak value of which was proportional to the duration of the flight data pulse. By suitable gating of the ramp voltages into peak voltage charging networks a continuous analogue voltage proportional to the data pulse width was produced for any desired channel.

However, as any speed changes occurring between record and playback produced variations in ramp height, the basic system was subject to an error which did not arise in the digital system. Since zero and marker (110%) signals were available, it was possible to automatically compensate for these errors.

Simple Analogue Output Voltage Generator

The principle of operation of the analogue voltage output generator may be studied with reference to the simple circuit of Fig. 76. In brief, the circuit charges capacitor C to the peak value of the ramp voltage of the particular channel selected. As the ramp height is proportional to the flight data pulse width, a voltage signal proportional to the value of the recorded parameter will appear across C. During the period between channel selector gate signals, the voltage at T17 is approximately zero and hence diode D1 will be reverse biased for negative going ramp voltages appearing at T8. However, when the negative going ramp channel selector gate voltage appears at T17, diode D1 will become forward biased and conduct via R_2. Similarly, D2 will now conduct and charging current will flow into C via R_2. If time constant R_2C is relatively short, the voltage across C will follow the ramp voltage at T8. When the channel selector gate voltage switches back to zero, both diodes D1 and D2 will become reverse biased and C will discharge with time constant R_1C via R_1. Diodes D1 and D2 will normally conduct only near the peak of the incoming ramp signal as capacitor C discharges to a relatively small extent between successive data samples for the selected channel.

In Fig. 77 a typical analogue voltage signal has been drawn for the circuit of Fig. 76. To prevent loading of the ramp output, R_2 should not be made too small. In the *Practical Analogue Output Voltage Generator* a value of (R = 56K) has been chosen (see Fig. 78 to be examined below). For capacitor C to charge at the input signal ramp rate, the required input current is kC where k is the ramp slope (300V/sec approximately). At the peak value of ramp voltage (–10V approximately), the current through R_2 will be at its minimum value of about 110 μA. Hence, for the voltage across C to follow the input ramp, C should be less than 0.37 μF (110/300). Note that any excess current through R_2, that is not required for the charging of C, flows via diode D1 through the ramp generator output circuit. When the input ramp voltage returns to zero, the voltage across C will begin to discharge towards zero voltage with time constant R_1C.

The above discharge time constant should be long compared with the repetition period of data samples for a particular channel. As the repetition period of the data samples is-1/3 second, a figure of (R_1C = 5 second) is suitable. Under these conditions about 7% peak to peak ripple voltage will appear on the basic analogue voltage output. For (C = 0.25 μF which as indicated above needs to be less than 0.37 μF), the required value of R_1 is 20 M. Such a resistance figure is quite impractical for most graphical recorders and hence a more complex system employing impedance buffering amplifiers had been used (refer to next section).

Practical Analogue Output Voltage Generator

For the simple circuit of Fig. 76, described in the previous section, there are many undesirable features. It was shown that for capacitor C to charge at the input ramp rate, it should have a value less than 0.37 µF. Using a capacitor C of value 0.25 µF would mean that a discharge resistor of value 20 M would be required to provide a 5-second discharge time constant. Such a value of discharge resistance is very inconvenient. Moreover, the resulting 7% peak to peak ripple at 100% signal level is somewhat excessive. In the simple circuit the rate of discharge of capacitor C, and hence the maximum rate at which the analogue voltage will respond to changes in sampled parameter value, will depend on the analogue signal level. For instance, it would take considerably longer for the analogue output to drop from 20% to 10% value than from, say, 100% to 90% value. To overcome these problems associated with the simple analogue voltage circuit, a more complex circuit as presented in Fig. 78 has been used.

To maintain a relatively long discharge time constant, of the order of some seconds and at the same time reduce the value of the discharge resistor, the diode D2 of the simple circuit of Fig. 76 may be replaced by the transistor Q707 as shown in Fig. 78. In this way capacitor C705, which replaces capacitor C of the simple circuit, may be increased in value. For a common emitter current gain of typically about 25 for transistor Q707, the capacitance as seen at the base of Q707 would be approximately 0.2 µF (5M/25). As the voltage drop across forward biased diode D708 and the voltage drop across the forward biased emitter base diode junction of Q707 are approximately equal during charge of C705, the peak voltage at the emitter of Q707 will be very nearly equal to the peak value of the selected ramp voltage. Variations in the diode voltages due to temperature changes should tend to cancel each other to a large extent in this arrangement. To enable capacitor C705 to discharge at approximately the same rate over the full range of ramp input voltage, capacitor C705 and associated resistor R722 have been returned to the positive supply line. In this way, capacitor C705 will discharge via R722 towards +24V between ramp charging pulses. The time constant of this discharge network is 6.5 second.

If any loading or filtering effect at the emitter of Q707 by way of C706 and R724 is neglected, the performance of the R722-C705 discharge network may be readily evaluated. The following equations enable the discharge voltage magnitude to be calculated.

$$v = (24 - v_R)\, e^{-\frac{t}{T}} = \frac{(24 - v_R)}{e^{\frac{t}{T}}}$$

where v is the voltage drop across R722-C705 at the end of the discharge period, v_R is the ramp height., T is the time constant of the discharge circuit and t is the discharge time.

For (t = 1/3 sec) and (T = 6.5 sec) $\frac{t}{T}$ equals 0.0512 and $e^{\frac{t}{T}}$ equals 1.0525.The value of v will vary with ramp peak value. For the marker channel ($v_R = -10$ V), (v = 32.30) and the discharge voltage drop will be (34.0 – 32.3) which equals 1.7 V (17% of maximum analogue signal) approximately. For the zero channel ($v_R = -0.8$ V), (v = 23.56) and the discharge voltage drop will be (24.8 – 23.6) which equals 1.2 V (12% of maximum analogue voltage) approximately.

Note that if the voltage on the emitter of Q707 rises to about 0.5 V the emitter base junction will begin to conduct and the voltage at the emitter of Q707 will become clamped to the zero-voltage output at T17 between channel selector gate signals. Under these conditions a marked non-linearity in the analogue output voltage characteristic would result. Although a

considerable increase in ripple is produced at the emitter of Q707 over that for the case in which C705 and R722 are returned to common, a significant improvement in the speed of response of the analogue voltage results.

As indicated in the previous paragraph, the ripple appearing on the analogue signal at the emitter of Q707 varies from 17% for the marker signal down to 12% for the "zero" signal (where percentages are expressed with respect to the peak marker channel signal). Obviously, such high ripple levels are unacceptable in the final analogue output. Now the most significant ripple component is the fundamental, having a frequency of 3 Hz. The ripple is, however, fairly rich in both even and odd harmonics, hence components at 6 Hz, 9 Hz, 12 Hz, etc., appear. To attenuate the fundamental to a very low value, a parallel T notch filter tuned to 3 HZ has been incorporated. The filter comprises components C706, C707, C708, R724, R725 and R726 as shown in Fig. 78. Capacitor C709 provides attenuation of the harmonics of the ripple frequency. Further analogue signal filtering and attenuation is achieved via R727 and the switched damping capacitor bank which is mounted on the front panel of the GSU. As most of the ripple has been attenuated by the time the analogue signal arrives at the damping switch, very little change in analogue signal will result as the amount of damping is varied. The variable damping allows the speed of response of the analogue output to be varied.

The impedance level of the analogue signal appearing at the wiper of the damping switch S102 is quite high (some megohm). To reduce the analogue signal impedance level to a figure which will render the output suitable for most graphical recorders, a triode valve cathode follower is used as an impedance buffer. The attenuation of the analogue signal between the emitter of Q707 and the grid of V701 may be trimmed via R729. Nominally the analogue voltage at the grid of V701 should be approximately 2/3 of the analogue voltage at the emitter of Q707. V701 is a miniature type EC70 triode which operates satisfactorily from the low voltage supplies used for the transistor circuits. It is extremely important that grid current in V701 be kept very low. Since grid current is not likely to be a very stable quantity it will produce a variable shunting effect on the grid resistor (series combination of R728 and R729) which in turn will cause analogue voltage fluctuations at the output. If the error due to grid current is to be kept less than 0.25% of full scale, the grid current variation must be kept below about 0.01 μA (assuming a 5V difference in analogue voltage output between 100% signal and 0% signal). Suitable choice of the plate current in V701 by adjustment of R731 enables the grid current to be reduced below 0.005 μA.

The cathode follower gain is approximately 0.93 and the output impedance as seen at the analogue output terminal T19 is of the order of a few hundred ohms. If the marker ramp signal is set to approximately –10V peak, a swing of about 5V in the negative sense should be obtainable at the output as the data input changes from 0% to 100%.

At the time the voltage analogue circuit was designed, the hybrid circuit was considered the simplest method of obtaining the low impedance output. However, it is to be understood that the same function is well within the ambit of semiconductors. An equivalent transistorised buffer amplifier would require more components, both active and passive. It was envisaged. at the time of the design of the decoder, that the analogue portion of the data decoder would later be extended to provide analogue voltage signals from each channel simultaneously as described in Appendix 9. With that extension in mind, the additional circuit complexity of a transistorised buffer amplifier represented a slight disadvantage. However, the recent advent of the field

effect transistor to the semiconductor market at the time when the GSU was developed, would almost certainly have meant that a different approach would have been available.

The chart recorder, which has been used most extensively for graphical recording of the analogue outputs, is a single channel potentiometric type having a full-scale sensitivity of 10 mV (Speedomax Type). To use such a recorder, the analogue output appearing at T19 is suitably attenuated by the circuit of Fig. 79. Potentiometer R104 provides zero adjustment so that the equivalent "zero" signal may be set to the edge of the chart grid. Adjustment of potentiometer R105 enables 100% signal to be set to a full chart width. In the design of the analogue voltage circuit, it was felt that a large amplitude analogue voltage swing (5V approximately) at a fairly low impedance level would be capable of driving most graphical recorders which might be used.

Overall analogue voltage output linearity can be readily assessed in the chart recording presented in Fig. 80. In this recording, taken with a Speedomax Recorder, the analogue output has been plotted as a function of data channel count (frequency doubled). "Zero" signal corresponds to 20 counts and 100% signal corresponds to 220 counts. The linearity was approximately 1.5% of full scale.

It is to be emphasised that the analogue voltage circuit responds more rapidly to an increase in signal than to a decrease. If, due to temporary desynchronization, a channel of much lower signal reading than the selected channel is wrongly gated into the analogue voltage circuit, very little change in analogue output signal will result, as Q707 will remain off during the presence of the gate signal. On the other hand, if a channel of much higher signal reading than the selected channel is wrongly gated into the voltage analogue circuit, C705 will rapidly charge to the higher signal level, but may take a considerable time (about 2 second if the marker is wrongly gated to the "zero" channel) to discharge to the normal level corresponding to the channel selected. Hence, it is imperative that desynchronization of the decoder be eliminated as far as possible for proper operation of the analogue voltage circuit.

The armature of switch S105 in Fig. 78 is shown connected to common. For automatic zeroing, to be discussed later, the armature is switched to the "zero" amplifier output terminal T22. S105 is a simple "on/off" switch which is accessible from the front panel of the GSU.

Automatic Zeroing

The analogue output voltage signals comprise a "zero" component common to all channels, and a signal component which varies from channel to channel and is proportional to the value of the parameter sampled in the recording process. The "zero" component arises because zero signal is made equivalent to 10 cycles of the 3500 Hz carrier. Automatic zeroing may be performed by subtracting from the normal voltage analogue an appropriate zero signal derived from the channel connected at all times to equivalent zero signal (Channel 7).

Let the total analogue voltage signal (average component) appearing on the emitter of Q707 in Fig. 75 be denoted by $(e_s + e_z)$ where e_s is the signal component and e_z is the "zero" component. By voltage divider action, the voltage at the grid of the buffer amplifier stage employing V701 will be some fixed fraction of the average voltage at the emitter of Q707. For simplicity, denote the voltage divider resistors by the symbols R_1 and R_2, where R_1 is the sum of the resistances of R724, R726 and R727, and $R2$ is the sum of the resistances of R728 and R729 (see Fig. 75).

The system of automatic zeroing may be studied with reference to the basic schema drawn in Fig. 78. Basically, it is required that the output voltage e_0 from the signal channel analogue voltage be some constant multiplied by e_s. If a separate analogue voltage circuit is produced for the "zero" channel and the output is amplified and fed to the lower end of resistor R_2 of the signal channel analogue voltage, as shown in Fig. 78, then the output e_0 will be given by:

From Fig. 81

$$e_x = \frac{A_1 A_2 R_2}{R_1 + R_2} e_Z$$

$$e_0 = \frac{e_x G_2 + (e_s + e_z) G_1}{G_1 + G_2} A_3 \; where \left(G_1 = \frac{1}{R_1}\right) and \left(G_2 = \frac{1}{R_2}\right).$$

Appendix 4 shows the use of conductance simplifies network analyses.

$$e_0 = \frac{e_x R_1 + (e_s + e_z) R_2}{R_1 + R_2} A_3$$

$$= \frac{A_3 R_2}{R_1 + R_2} e_s + \frac{e_Z R_2 + e_x R_1}{R_1 + R_2} A_3$$

If $(A_3 = A_1)$ $then$:

$$e_0 = \frac{A_1 R_2}{R_1 + R_2} e_s + \frac{A_1 R_2}{R_1 + R_2}\left(1 + \frac{A_1 A_2 R_1}{R_1 + R_2}\right) e_Z$$

$$\text{and if } \left(1 + \frac{A_1 A_2 R_1}{R_1 + R_2} = 0\right)$$

$$e_0 = \frac{A_1 R_2}{R_1 + R_2} e_s$$

which is of the form required.

Hence the requisite gain of the zero amplifier is given by

$$A_2 = -\frac{1}{A_1}\left(1 + \frac{R_2}{R_1}\right)$$

The buffer amplifier gain A_1 is approximately 1 and $\frac{R_2}{R_1}$ is approximately 2.

Hence $A_2 \approx -3$.

The "zero channel" voltage analogue, referred to in Fig. 78, uses a circuit virtually identical to the one used for the signal channel analogue voltage drawn in Fig. 75, except that no adjustable components are incorporated. Complete details of the "zero channel" analogue voltage circuit are given in Fig. 79. Gating of the "zero channel" ramp is achieved by permanently connecting diodes D802, D803 and D804 to the *Binary Counter* outputs T11, T14 and T16 respectively in an "AND" circuit arrangement. The" zero channel" analogue output appears at T20 relatively ripple-free.

The circuit of the "zero" amplifier (referred to in Fig. 78) is presented in Fig. 83. The gain of the amplifier is feedback-stabilized to a figure of approximately –3. Setting of the gain is performed by adjustment of potentiometer R902, which changes the ratio of the feedback resistor value (value of R901 plus associated portion of R902) to the input resistor value (value of R903 plus associated portion of R902). R902 is mounted on the front panel of the GSU and is labelled as GAIN 2. When the gain has been appropriately adjusted, the zero may be set by adjustment of R910. In other words, R910 is set such that zero output is obtained with zero input. R910 is mounted on the front panel of the GSU and is labelled as O.P.→ZERO.

Automatic Calibration

The provision of a marker channel, which is connected to a fixed DC potential in the recording equipment, enables all channels to be calibrated. Any speed changes between record and replay of the data signal will effectively produce pulse duration changes in the data signal. Such changes, in turn, will produce changes in the analogue output. During record and playback of the wire recording, the head moves up and down vertically, with a repetition period of approximately 15 second, in such a manner that the wire winds evenly on or off the spools. At times, a noticeable wow component having a repetition period equal to that of the head traverse (15 second) appears on the analogue signals. As such speed variations produce proportional variations in the analogue output from each channel, it is possible to compensate for the variations on the signal channels by observing the variation on the marker channel. In the system to be described here, variations in the analogue output due to speed variations between record and replay of the wire recording are cancelled out to a large extent in a system of automatic calibration.

The basic principle of automatic calibration may be studied with reference to the block schema of Fig. 81. Due to difficulties encountered with hunting in a completely closed loop automatic calibrating system, such a system was abandoned. The system adopted employed a separate ramp generator and analogue voltage circuit for extracting the marker analogue signal. Variations in the marker analogue signal, due to causes outlined in the previous paragraph, will be inherent in the output signal from the *Marker Voltage Analogue* block (Fig. 81). The output from the *Marker Voltage Analogue* is compared with a fixed DC reference and the difference is amplified and fed back to the signal ramp generator in such a way as to cause the slope of the signal ramp to vary. By suitable selection of the differential amplifier gain the correct amount of compensation may be established.

Consider that, due to speed variations between record and playback, the duration of the data pulses is increased by a fractional amount ϵ. To assist in the analysis, the various signal levels throughout the automatic calibration circuit have been presented in the block diagram of Fig. 81 for a fractional increase in data pulse width of ϵ. If T_C. is the normal duration of the marker pulse, then, the input to the marker ramp generator may be written as $T_C(1 + \epsilon)$. The analogue voltage appearing at the output of the *Marker Voltage Analogue* block may be written as $K_1Tc(1 + \epsilon)$ where K_1 is a constant depending on marker ramp slope and attenuation within the *Marker Voltage Analogue* circuit. If the reference side of the differential amplifier is fed with the normal output voltage K_1Tc, then an output signal proportional to ϵ, actually $\epsilon\beta K_1Tc$, will be obtained from the differential amplifier where β is the differential amplifier gain. Now the slope of a ramp generator is proportional to the DC supply voltage. By subtracting the output of the differential amplifier from the ramp supply voltage V_{CC} and feeding the difference

voltage to the signal ramp generator, variation in the signal ramp slope is accomplished. Assume that the *Signal Voltage Analogue* is extracting a channel of input pulse duration nominally T but changed to $T(1+\epsilon)$ on account of a speed variation. The output voltage of the signal ramp generator circuit may then be written as $K_2(V_{CC}-\beta\epsilon K_1 T_C)T(1+\epsilon)$ where K_2 is some constant depending on the passive components in the ramp generator circuit. Potentiometer R914 (Fig. 85) allows the ramp slope to be trimmed which translates as a pulse duration trim. R914 is mounted on the front panel of the GSU where it is given the label O.P.→ATTEN.

Assuming that the nominal "zero" pulse has a width of T_0, then, by virtue of the speed variation, this width will be changed $T_0(1+\epsilon)$. If automatic zeroing is used in the *Signal Voltage Analogue* circuit, the final output $T(1+\epsilon)$will be given by:

$$e_0 = K_3(V_{CC}-\beta\epsilon K_1 T_C)(T-T_0)(1+\epsilon)$$

where K_3 is a constant depending on the value of K_2 and the attenuation within the voltage analogue circuit.

If $\beta K_1 T_C$ is made equal to V_{CC}, or in other words, β is made equal to $\frac{V_{CC}}{K_1 T_C}$, the following expression applies for e_0:

$$\begin{aligned} e_0 &= K_3 V_{CC}(1-\epsilon)(T-T_0)(1+\epsilon) \\ &= K_3 V_{CC}(T-T_0)(1-\epsilon^2) \end{aligned}$$

If ϵ is, say, a 5% variation then the error produced in this automatic compensating system will be reduced to ϵ^2 or 0.25%.

The circuit of the marker ramp generator is drawn in Fig. 85. It is very similar to the signal ramp generator drawn in Fig. 65 and described in Sec. 5.2.3.2.1.3. To prevent loading on the basic ramp generator circuit, the output is taken via an emitter follower to the marker channel analogue voltage circuit drawn in Fig. 86. Marker channel (Channel 8) gating diodes D806, D807 and D808 are permanently connected to the appropriate *Binary Counte*r outputs such that the marker channel is selected. Analogue signal attenuation and ripple filtering is virtually identical to that described for the *Signal Voltage Analogue* circuit in the *Practical Analogue Voltage* item examined above. The *Marker Voltage Analogue* output, appearing at T21 in the *Marker Voltage Analogue* circuit of Fig. 86, is fed to one side of the differential amplifier shown in Fig. 87. The other side of this differential amplifier is connected to a fixed DC reference and is adjusted via R918 to the normal output from the *Marker Voltage Analogue*. Circuit. R918 is mounted on the front panel of the GSU and has been given the label GAIN 1.The difference voltage is amplified by the differential stage comprising transistors Q907 and Q908. Coupling to the amplifier output by way of a pair of emitter followers, Q909 and Q910, enables a low impedance output suitable for feeding to the signal ramp generator circuit, to be obtained. Since Q909 and Q910 are NPN and PNP types respectively any changes in emitter-base voltage due to temperature variations will tend to cancel to a large extent. The output of the marker amplifier is returned to the signal ramp generator of Fig. 65 via the Auto-Cal. switch SI04B. In Fig. 88 the marker channel output as derived from the *Signal Voltage Analogue* circuit has been compared for the case of the automatic calibration operative and inoperative. Most of the low frequency wow component (having a repetition period of

15 second approximately) disappears with the automatic calibration operative. Unfortunately, the author has not kept a record of the vertical axis range relative to 100% signal range.

The overall accuracy obtainable using the analogue system of decoding is ±2% of full scale. By virtue of the recording system employed, the maximum accuracy obtainable with the most accurate decoding method (digital) is ±1 % full scale (or possibly ±0.5% under ideal conditions).

5.2.3.2.2.5 Possible Simple Extension of the Ground Station Unit (GSU)

The Flight Data element of the GSU had been designed for an 8-channel system employing a sampling rate of 24 input samples per second. If the sampling rate and the data carrier frequency (3500 hertz) were left unchanged and the number of channels were increased, very little modification would have been required for the GSU. The *Binary Counter* and the Channel Selector, described in Sec. 5.2.3.2.2.2 and Sec. 5.2.3.2.2.3 respectively, would have needed to be changed a little. By adding one additional bistable circuit to the *Binary Counter* and an additional section to the *Channel Selector* switch, up to 16 channels of data could have been handled. As a change in the number of channels under these conditions would mean a different sampling rate for an individual channel, some alteration would have been required in the voltage analogue filter circuits.

5.2.4 Power System for Ground Station Unit (GSU)

The following supplies are required for the Ground Station Equipment:

(i) +24V at 50 mA, regulated DC for various electronic circuits used throughout the Ground Station Equipment.
(ii) –24V at 100 mA, regulated DC for various electronic circuits used throughout the Ground Station Equipment.
(iii) 6-3V at 1.2A, unregulated AC for filaments of miniature valves used in buffer amplifiers in the flight data decoder section.
(iv) –32V at 850mA, unregulated DC of moderately low ripple for the speech power amplifier. The voltage specified is a nominal full load value chosen as a suitable level for the unregulated input to the –24V regulator.

On the assumption of a –32V input to the regulators, the total transformer secondary power requirement would be –32V at 1A (32 watt) plus 6-3V at 1.2A (about 8 watt). Hence power demand from the transformer secondary is about 40 watt. However, since a class B stage is used for the output of the speech amplifier, the above level of power would be reached only during bursts of speech, and the standby power requirement would be considerably less.

The power supply included some large components and was housed in a separate module (Fig. 89) in the GSU.

5.2.4.1 Power Transformer and Rectifier-Filter Unit

The regulated supplies and the –32V unregulated supply may have been conveniently derived from a centre-tapped secondary winding. As a suitable transformer was not readily available at the time of the design, the secondary of a Trimax TP 1684 transformer was extracted and rewound for this particular application. A centre-tapped winding having 27V R.M.S. nominal per side and a separate 6.3V winding were added. The primary of this transformer had 240V

and 210V tappings. As the power supply had been designed to accommodate a ±10% mains variation, voltages in the range 216V to 264V would be accommodated by the 240V tapping, and voltages in the range 189V to 231V would be accommodated by the 210V tapping.

A full wave rectifier with a single reservoir capacitor on each side for filtering provided unregulated DC of sufficiently low ripple for the speech power amplifier and for the inputs to the regulators. Circuit details of the power unit, comprising transformer, rectifier and filter is given in Fig. 90. The ripple on the –32V supply at full load was 1V peak to peak, and reduced to 0.25V peak to peak for zero signal in the speech channel.

5.2.4.2 –24 Volt Regulator

The circuit of the –24V regulator is drawn in Fig. 91. The series combination of the Zener diodes D210 (6.2V nominal) and D211 (4.7V nominal) serves as the voltage reference. B*y* suitably choosing the operating current in these diodes, a voltage reference with close to zero temperature coefficient was obtainable. A series connection of two Zener diodes, having the breakdown voltages specified, was used since the Zener voltage temperature coefficient changes sign about this level of voltage. Experimentally, it had been found that, at 3.2mA operating current, the combination of diodes used had a reference voltage which remained stable within ±4 mV as the temperature was varied from 0°C to 55°C. At room temperature and 3.2 mA operating current the reference voltage was 11.496V. Hence the reference voltage stability over the temperature range 0°C to 55°C was ±0.0035%. If the operating current was raised above 3.2 mA, the combination exhibited a positive temperature coefficient; if below, the combination exhibited a negative temperature coefficient. The incremental resistance of the combination at 3.2 m A was approximately 185 ohm. The resistance value of R221 was chosen to provide the required level of current in the Zener diodes.

The differential amplifier combination, Q209 and Q210 tended to stabilise the regulator with respect to transistor emitter-base voltage changes with temperature. As the collector current for the amplifying transistor Q208 was obtained from the unregulated input line, mains voltage variations would cause this current to change. In order to minimize current changes reflected back into the differential stage, a compensating resistor R214 was added. Its value was equal to R215 multiplied by the current gain (22 approximately) of transistor Q208. That gave the resistance value of R214 as 180 K. Ideally, any change in base current in Q208, as a result of mains voltage variations, flowed via R214. Emitter follower Q207, which drove the main series transistor Q206, provided an additional stage of amplification.

Short circuit protection of the regulator was provided by resistor R219 and diode D209. Under normal conditions the voltage across silicon diode D209 was so low as to render it virtually non-conducting. If an overload occurred on the output of the regulator, the increased current through R219 would cause a voltage drop which, when added to the emitter-base diode voltage of germanium transistor Q206, would cause D209 to conduct, hence limiting the current in Q206. In Fig. 92 the collector current of Q206 has been plotted as a function of drive current (base current of Q206 plus current through D209) for R219 equal to 3 ohm. Above about 150mA the collector current limiting action becomes apparent. R216 limits the available drive current to approximately 50mA (for Q207 saturated and assuming 32V unregulated input). Hence the short circuit current through the main series transistor cannot exceed about 250mA (see Fig. 92). The measured value of short circuit output current in this regulator $(I_C + I_D)$ at 32V input was 295mA, a value which was reasonably close to the design figure above.

Capacitor C204 had been added to remove the tendency of the regulator to oscillate at high frequency. Capacitors C205 and C206, apart from assisting to reduce the tendency for oscillation, reduced the output ripple to a low value. The following measurements were made on the –24V regulator at a nominal mains voltage of 240V and an output current of 100mA.

Output Impedance = 0-012 ohm.

Stabilisation Ratio defined here as $\left(\frac{\%\ change\ in\ mains\ voltage}{\%\ change\ in\ regulated\ output\ voltage}\right)$ = 5350.

Output Ripple = 0.2 mV peak-to-peak for resistive load, 1 mV peak-to-peak for actual load.

5.2.4.3 +24 Volt Regulator

Referencing of the +24V supply was achieved using the –24V regulated output. Using such an arrangement drift in the basic reference diodes would cause both supplies to drift in unison, which in turn would tend to produce error cancellation in some of the GSU circuits.

The complete circuit of the +24V regulator is drawn in Fig. 93. Apart from slight modifications in the differential amplifier stage due to the different method of referencing, the circuit is a direct analogue of the –24V regulator with the PNP transistors replaced by NPN type. The design considerations mentioned with regard to the –24V regulator also apply here.

Two silicon diodes, D206 and D207, were used for short circuit protection purposes. The additional diode was required in this circuit because the main series transistor Q201 was a silicon type. At 32V input, the measured value of short circuit output current in this regulator was 200 mA.

Capacitor C203 served to reduce the output ripple.

The following measurements were made on the +24V regulator at a nominal mains voltage of 240V and an output current of 50mA.

Stabilisation Ratio defined here as $\left(\frac{\%\ change\ in\ mains\ voltage}{\%\ change\ in\ regulated\ output\ voltage}\right)$ = 1500.

(The variation in the –24V regulated output as a result of mains voltage variation is partly the reason why this ratio is lower than that for the –24V supply.)

Output Ripple = 0.2 mV peak-to-peak for resistive load, 1.5 mV peak-to-peak for actual load.

5.3 Review of Flight Memory System Data Recovered from the 23-March-1962 Flight Test

All previously documented Flight Memory System electrical circuit development was completed before clearance for a flight test was given. The flight test was arranged with the assistance of the Department of Civil Aviation (DCA) which provided aircraft and aircrew for the test. The test occurred on 23-March-1962 in DCA's Fokker Friendship aircraft with Charlie-Alpha-Victor (CAV) call sign. The aircraft was flown from Essendon airport to Avalon (without landing) and back to Essendon. Members of the Flight Memory development team on-board included Dr Warren, Mr Sear and the author. Flight Memory data were recorded via the airborne magnetic wire reorder.

Subsequent to the test flight, the complete flight recording was copied to a Rola Model 66 magnetic tape recorder for ease of handling multiple passes of the retrieved signal (necessary for the ground system analysis). The output from the magnetic tape recorder formed the input to the Ground Station Unit (GSU). Refer to Fig. 55 for details of the interconnection of the GSU and external processing equipment. Selected samples of the externally processed data were recorded on paper media. In each case the paper record was photographed and annotation was added to the photograph.

Fig. 91 presents some high speed oscillograms which were taken using an ultra-violet recorder (author has not retained device Make and Model details). The upper trace shows a sample of the composite signal appearing on playback prior to any filtering, and the middle and lower traces show the filtered speech and flight data components respectively. In the case of the Flight Data component, samples of marker, altitude, airspeed, pitch and roll are presented 1/24th second apart. The finite build-up and decay times of the filtered data can be observed. Amplitude variations inherent in the record/playback process are in evidence on the envelopes of the filtered flight data. The Flight Data UV plot is similar to the idealised one of Fig. 61 referred to in the *Frequency Doubler* Sec. 5.2.3.2.1.1.

In Fig. 95 a photograph of the Ground Station, comprising the GSU and various commercial units (the UV recorder has been omitted) is provided. Labels have been added to the various devices for the photograph shoot in what was an exhibit rather than a working arrangement. The output of the Rola Model 66 tape recorder was fed to the GSU's HI input. The Hewlett Packard Type 522B Electronic Counter and associated Hewlett Packard Type 562A Digital Recorder, on the top left of the photograph, were used for automatic digital presentation of Flight Data, one channel at a time. Analogue presentation and plotting of audio and flight data were made possible with the addition of the Speedomax (l0mV full-scale) potentiometric recorder shown on the extreme right of the photograph.

No record is available of the single-channel-at-a-time output from the Hewlett Packard Digital Recorder. That approach was adopted for recording the digital counter output. The Hewlett Packard Digital Recorder output of simulated data to illustrate what was at the time a proposed extension to provide a simultaneous readout of all channels by that Recorder is provided in Fig. 96.

The original full-flight duration analogue recording automatically plotted with the aid of the Speedomax recorder moving at 0 5 inch per minute, is shown in Fig. 97. Such a record gives an overall picture of a complete flight and would normally be taken as the first step in an accident investigation. Signal plot crossover was achieved by plotting the signals one at a time with care to insure the start point of each plot was at the same tape replay instant. A colour copy of the analogue *Flight Data* for the 23-March-1962 full flight was made as part of an exhibit for ARL's 60th anniversary in 1999. A photograph of that copy is provided in Fig. 98.

For finer resolution of any portions of interest, a higher speed recording may then be taken. A sample of the original recording that was taken at a chart speed of 6 inch per second is shown in Fig. 99. In that figure a simulated emergency descent started at approximately the 37-minute-mark is illustrated. Cockpit speech available from the output located at extreme lower right of the GSU front panel has been recorded concurrently with the flight data on the upper edge of the chart. In this way motion of the aircraft may be associated timewise with any comment made by a member of the crew. From the Reference (Marker) Channel graph it is evident that

AUTO-CAL was switched off when this graph was plotted. A near-copy of the above plot was made as part of an exhibit for ARL's 60th anniversary in 1999. A photograph of that copy is provided in Fig. 100.

Part D: End Items

6. Other Contributions

All previous Sections in this document have been mainly of a scientific or technical nature (predominantly electrical) in relation to the Flight Memory invention. Most other contributions, which are publicly available, are mainly historical in nature such as what the contribution was, when it happened and who was involved. A selection of some of the main contributions will be outlined here.

An eight-item selection of the main items will be outlined in the list order below.

1. Author's Website
2. Flight Memory Summary Document
3. Other Documents
4. Book by Janice Witham
5. Photographs
6. Lawrence Hargrave Award
7. Films & Audio
8. Stage Play

6.1 Author's Website

Included at the author's website is a page (https://www.kenblackbox.com/blackbox.htm) assigned to the Flight Memory system (under the Black Box name). That page is dynamic as the topic has acquired perennial interest with the next update always awaiting action. Updates include HTML notes, PDF documents, photographs, films etc. When complete, this document will be made publicly available from the author's website defined above. A younger close friend has offered to maintain the Black Box page updates after the author's passing.

6.2 Flight Memory Summary Document

A document which summarises the Flight Memory history and the 1962 flight test results was written by Dr Warren and the author in 1998.

6.3 Other Documents

There are many documents relating to the Flight Memory system that have been produced. Most are available in PDF form at the author's website. A full list of is included in the Reference list at the end of blackbox.htm page mentioned above. A selection from that list will be mentioned here.

1. The first official document (Ref. 1) by Dr Warren to outline his aircraft accident recording concept was produced in 1954 with an April date.
2. Documents (mainly correspondence) referring to the development of the Australian Black Box voice-plus-data recorder: National Library of Australia Archives with unique identifier Bib ID 139608. The document comprises a batch of about 860 pages of A4 size in two volumes and was passed to the National Library on 16 Dec 1999. Volume 1 applies to the period 1953 to 1962 and Volume 2 to 1963 onwards. Copies are held by the Warren family and the author.

3. Mr Sear's grandson, Jeremy, produced "The ARL 'Black Box' Flight Recorder - Invention and Memory", Thesis Ref. 14567 for Bachelor of Arts (Honours), Department of History, Faculty of Arts, The University of Melbourne, October 2001. That document was in HTML format and was later converted by the author to a PDF format so that text and images were combined in a single document.
4. Bill Schofield, "Bill Schofield's Hargrave Memorial Lecture", 6 December 2010.
5. Australian Government Civil Aviation Authority, "The dawn of the black box", Flight Safety Australia magazine, January - February 2013 edition.
6. "David Warren, Inventor of 'Black Box,' Dies at 85". This article provides a summary of Dr Warren's life with particular reference to the Black Box invention.

6.4 Book by Janice Witham

"Black Box", Janice Witham, February 2005, 215 pages, published by Thomas C. Lothian Pty Ltd, 11 Munro Street, Port Melbourne, Victoria, 3207. Dr Warren's younger daughter Jenny Warren is a good friend of Janice and, no doubt, had input to and influence on the selection of the topic for this book. At the time of writing copies of the book are not available for sale. Copies are held by the Warren family, the author and others

6.5 Photographs

Because of local and international interest by film makers and others, the author receives numerous requests for higher quality images relating to the Australian black box and the participants in its development. In most cases there is a scarcity of good quality images taken around the time of the early developments. A list of the best available images with a brief description of each entry, with year of creation where possible and a link to the image, has been made publicly available. Because of the perennial interest in the Australian black box topic and the associated new photographs that arise, there is a never-ending demand to add items to the list.

6.6 Lawrence Hargrave Award

Dr Warren, together with the team involved in the pre-production 1962 Flight Memory prototype development, were recognized in the Lawrence Hargrave Award granted by the Australian Division of The Royal Aeronautical Society in February 2001 (almost 40 years after the successful flight demonstration occurred). The award was presented by The Hon John Anderson MP, who was the Australian Minister for Transport at the time. A photograph of the award is available.

Dr Warren was the recipient of many other awards. Go here for the full list.

6.7 Films & Audio

At the time of writing, three main films relating to the Australian Flight Memory aircraft accident recording system had been made:

1. Warren-1962-film: Australian Government Department of Supply ARL Black Box 8 min 39 sec film produced in 1962 after the successful 23 March 1962 black box concept demonstration flight. Dr Warren provided the voiceover. (Size 132 Mb, Length 8 min 32 sec).

2. Smithsonian-1990-film: Pay TV Discovery Channel: Invention Episode 5 (second item) "Black Box", Smithsonian Institution presentation, copyright 1990. The duration of the ARL Black Box segment is 5 min 10 sec. Film production for the ARL segment was performed by the Beyond International Group in 1990. (Size 79 Mb, Length 5 min 10 sec).
3. Northern-Pictures-2019-film: This film is an edited "Black Box" portion of Australian film produced by Northern Pictures (a film production company with headquarters in Sydney). The unedited film named as "Aussie Inventions That Changed The World: S1, Ep7. Airborne:" was shown on ABC free-to-air television on 14 April 2021. The complete film duration was 79 min and that of the "Black Box" portion was 21.6 min. The size of the edited portion was 2.05 GB. The complete film was first shown on 5 Aug 2019 via Foxtel Pay TV "Episode 7: Airborne" of an eight-episode series named "Aussie Inventions That Changed The World".
4. BBC Witness podcast "BBC-2015-podcast" on 23-Mar 2015 that includes interviews with Jenny and David Warren (children of Ruth and David Warren). Size 4.3 Mb, Length 9.0 min.

6.8 Stage Play

A Stage Play based on the Australian Flight Memory (Black Box) invention was presented at the Street Theatre in Canberra, Australian Capital Territory (ACT) in November 2019. It was a production of playwright Alana Valentine that presented a narrative song cycle about Australian genius. It used the Flight Memory development as an example of how Australia treats its scientists. Click here to view photographs taken on the premiere opening night.

7. Influence of Australian Flight Memory System on Local and Overseas Markets

Two items are considered in this section.

1. Recognition of Dr Warren as Black Box Inventor
2. Flight Memory Related Black Box Developments Locally and Overseas

7.1 Recognition of Dr Warren as Black Box Inventor

Dr David Warren is widely regarded as the inventor of the Black Box system that forms the closest match to the Black Box systems that are now commonplace in airplane and other applications. The Institute of Electrical and Electronics Engineers (IEEE) is probably the highest ranked body to recognize (Ref. 20) Dr Warren as the inventor of the black box systems which have been in common international use since the 1970s. The IEEE is the world's largest technical professional organization dedicated to fostering technological innovation and excellence for the benefit of humanity. Its reach extends beyond its original electrical and electronic fields. Actual quotes from an IEEE Spectrum item (Ref. 21) include: "The original black box was designed by David Warren of Australia" and "The black box may be the greatest single invention in the history of safety engineering".

Dr Warren named his invention as the Flight Memory system and that unique title will be used here when referring to his system. Two versions of the Flight Memory system were produced and the author has referred to these as The Mk 1 and Mk 2 systems. The Mk 1 was validated in 1958 and the Mk 2 in 1962. The Mk 2 was a significant improvement on the Mk 1 and

provided convenient Cockpit Audio and Flight Data outputs that would be suitable for detailed analysis by accident investigators.

The Mk 2 Flight Memory system was built as a pre-production item but it never entered service. After the 1962 validation flight, it was assumed by Dr Warren and the electrical design team that some further development activity would proceed before a manufacturer was identified. It turned out that no further local development took place.

7.2 Flight Memory Related Black Box Developments Locally and Overseas

In January 1963 Australia was the first country in the world to make CVRs mandatory. The Minister for Civil Aviation announced in March 1961, that technical developments (as observed in the Flight Memory development) enabled his department to require the installation of flight recorders in airlines. Each recorder was to have a device to erase all recordings of cockpit conversations at the conclusion of a successful flight by January 1963. The cockpit voice erasure requirement as stated is not required in modern recorders. Standard practice in the early days was to automatically overwrite in a continuous loop of typically 0.5 hour of audio and 2.0 hour of flight data.

To meet the mandatory requirement Australian airlines decided to contract American United Data Corporation (UDC) to provide flight data and voice recorders to meet the Department of Civil Aviation (DCA) requirement. That contract effectively ruled out any local development of a production model of the Flight Memory system.

In 1963 in anticipation of the coming British Ministry of Aviation (MOA) accident recording mandatory requirement, the British firm S. Davall & Son approached ARL for the production rights for the ARL system. In August 1963, Davall who had hopes of gaining a contract to produce a system based on the ARL Flight Memory Cockpit Voice and Flight Data recording and recovery system, sought production rights for the Flight Memory system. The MOA defined a mandatory requirement that included flight data but not cockpit audio. British European Airways (BEA) contracted Davall to make the recorder but the electronics contract went to Plessey. The Davall "Red Egg" accident recorder, based on the ARL system, used magnetic wire as the recording medium, and was in production over the 1968 to 1978 period. It won a large part of the British and overseas market at that time. Cockpit voice recording did not become mandatory in England until after the "Staines disaster" on 18 June 1972 when BEA Flight 548, on a scheduled passenger flight from London Heathrow airport to Brussels, crashed soon after take-off, killing all 118 people on board.

7.3 Comparison of Australian Flight Memory System with Later Black Box Versions

Although many technical advances have occurred since the first commercial cockpit voice plus flight data recording system was fitted in an airplane, the basic functionality has changed very little. Ref. 22, written by the author, includes a comparison of the Flight Memory system with the modern-day derivatives. The following table copied from that reference compares the Warren Flight Memory invention with those that came into service from the mid-1970s onwards.

Property	Present day device capabilities	Warren device capabilities
Recorded information	Cockpit audio	Cockpit audio
	Flight data	Flight data
Information storage	Endless-loop principle (overwrite earliest data)	Endless-loop principle (overwrite earliest data)
Information survivability	Impact-proof	Impact-proof (not tested)
	Fireproof	Fireproof (confirmed via test)
	Waterproof	Waterproof (would need to be impact-proof before being considered - not tested)
Locator	Underwater Locator Beacon (ULB)	Not provided
	On-land Emergency Locator Transmitter (ELT)[a] external to current black boxes	Not provided
Position in plane	Tail (offers best chance of survival)	Tail recommended in 1954 by Dr Warren
Automatic switch-off of recording on normal landing or after crash	Provided on normal landing and assumed to apply after a crash	Not provided[b]
Continued recording if power failure occurs	Not provided	Provided[c]
Deployable option[d]	Fitted in some helicopters	Deployable option was under consideration

a. The fitting of ELTs on planes is standard and the associated antenna requirement means they need to be fitted near the skin of the aircraft and not where the black box hardware is normally placed. Emergency locator transmitters (ELTs) are small battery-powered devices that broadcast a distinct sound on a dedicated emergency frequency. Older units broadcast on the emergency frequency 121.5 MHz, while newer models broadcast on 406 MHz.

b. Automatic switch-off (like ULB switch-on) was not provided on impact deceleration in the Flight Memory system to prevent overwrite. Such a switch would be desirable so as not to depend on the connection between the two airborne boxes being severed when the crash occurred. This was among the extra features that would have been investigated if further development had not ceased after the 1962 system validation flight.

c. The Australian airborne power system (Sec. 4.3) was of significant complexity. It included a 24 V chargeable battery. Under normal operating conditions it drew power from the standard aircraft 28 VDC supply. The recorder motor was a three phase type (200 VAC phase-to-phase or 115 VAC phase-to-neutral). It was a 400 Hz four-pole hysteresis type which ran at synchronous speed (1200 RPM). It also provided DC power for the Electronics Unit. The overall power required was 25 watts.

d. While deployable recorders are not currently in use on fixed-wing passenger planes, they are in use on some helicopters. In effect they are meant to eject the black box with built-in CVR and FDR when predetermined triggering conditions are met. They carry a radio beacon and their buoyancy enables them to float on water. Some believe they should be fitted in fixed-wing passenger planes. While no tests were performed on a deployable unit for the Flight Memory system, the idea was in the forefront of those being investigated by Dr Warren. A detachable recording medium within a foam plastic aerofoil and fitted with a radio beacon transmitter was one such possibility under review. It was based on a type that had been developed by the National Research Council of Canada.

8. Concluding Remarks

1. The main aim of this document, which was to describe to the extent possible all electrical circuits for the 1962 flight-verified Flight Memory system, has been achieved.
2. Additional items examining *Other Contributions* and *Influence of Australian Flight Memory System on Local and Overseas Markets* have been included.
3. This document is intended as a reliable single source of the electrical aspects of the 1962 flight-verified Flight Memory system.

Acknowledgements

The author wishes to acknowledge:

1. Major contributions to this document by written and other work by deceased members of the 1962 Flight Memory system design team, Dr David Warren, Mr Lane Sear and Mr Walter Boswell.
2. Contributions to the testing in 1961-2 of the Flight Memory ground station processor by ARL employees Mr J. Goldman and Mr G.H. Wain.
3. Major contribution by Mr Domenico Lombardo, a retired aeronautical scientist from the renamed ARL site, in the production of images for and the vetting of this document.
4. An offer by Mr Lombardo, gratefully received by the author, to be the custodian for the author's website, which includes a page devoted to the Flight Memory system, when the author can no longer manage that.

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A2 Sander Sloots; Loud mole crickets Surrey Hills Melbourne, 2 April 2017: and song.

A3 Brisbane Mole Cricket background and song.

A4 Common Mole Cricket and Calling Songs.

A5 "Documents (mainly correspondence) referring to the development of the Black Box voice-plus-data recorder", National Library of Australia Archives, Bib ID 139608, The document comprises a batch of about 860 pages of A4 size and was passed to the National Library on 16 Dec 1999.

A6 Massachusetts Institute of Technology, Understanding Poles and Zeros, Department of Mechanical Engineering, 2.14 Analysis and Design of Feedback Control Systems.

A7 Swarthmore College: Linear Physical Systems Analysis; Table of Laplace and Z Transforms.

Appendices

Appendix 1: Amplifier Basics

Amplifiers under consideration provide an output voltage V_{out} that is higher than the input voltage V_{in} by some multiple k: ($V_{out} = kV_{in}$). That sounds simple but the analysis of their operation can be significantly complex. For the Airborne Electronics Unit and the Ground Station Unit the amplification of static or slowly changing inputs is not required, so AC coupling via capacitors can be used. That represents one simplification.

The open loop gain of transistor amplifiers varies considerably between devices and also with temperature. It follows that nearly all amplifier circuits use feedback to stabilise their gain. That means they are, in effect, control systems that need care to avoid instability. As a general rule, for an amplifier with a nominal open loop gain of 100, the author would set the closed loop gain (i.e. with feedback) to no greater than 10.

In 1961 (the year when most of the Flight Memory development occurred) silicon NPN transistors were the normal choice for airborne-quality low power applications.

The simplest single-stage NPN transistor amplifier is one with a single input and an inverting collector output. A single-stage non-inverting emitter-output NPN transistor amplifier variant is also possible. Two-stage similar amplifiers produce a non-inverting output. Single- channel (non-stereo) signals apply for the audio signals in the Flight Memory application and inversion has no effect on the output sound.

Amplifier feedback, apart from providing gain stabilisation, produces greatly increased input impedance and greatly reduced output impedance.

To demonstrate some basic configurations, two amplifier circuits which have been used by the author will be considered.

Pre-Amplifier Used in Flight Memory Ground Station Unit

A complete analysis of this amplifier is provided in Ref. 8 (page 4). The amplifier circuit is reproduced in Fig. A1-1 (which is a reproduction of Figure 5 of that document). A 2-stage amplifier is used and its gain is close to the value of R_F divided by R_E which in this case is 68.

Microphone Output Amplifier Used in Some Flight Tests

A complete analysis of this amplifier is provided in Ref. A1. The amplifier circuit is reproduced in Fig. A1-2 (which is a reproduction of Figure 4 of that document). The microphone typically generates a 2.5 millivolt (mV) peak output level and requires amplification to raise the amplified output to 1.4 V. A 3-stage amplifier is used and its gain is close to the value of feedback resistor R_6 divided by R_1 which in this case is 560.

Appendix 2: Cockpit Voice Processor Stop Band Attenuation Slopes

A figure-of-merit for filters is the stop band attenuation in the region below the 3 db cut-off frequency (from about 6 db down). While a detailed analysis of the High Pass and Low Pass Filter circuits may provide estimates of the stop band attenuation slopes that would be very complex. Furthermore, it would not be required as the frequency response of the Band Pass Filter has been plotted (Fig. 14). For comparison purposes a simple RC filter provides 6 db/octave stop band attenuation slope. In the following calculation the db/octave will be estimated. To convert to the other commonly used db/decade, the relationship 20 db/decade equals 6 db/octave approximately can be used. In other words 1 db/octave equals 3.33 db/decade.

A frequency ratio expressed in octaves is the base 2 logarithm of f_2/f_1 where f_1 is the lower frequency: $log_2\left(\frac{f_2}{f_1}\right)$.As logarithm tables for base 10 are far more common than those for base 2, it is convenient to use the general conversion: $log_b(x) = \frac{log_d(x)}{log_d(b)}$.

For the base 2 to base 10 conversion: $log_2(x) = \frac{log_{10}(x)}{log_{10}(b)}$.

Substitute $\frac{f_2}{f_1}$ for x in the following calculations.

High Pass Filter

From graph (Fig. 14) we have 16 db attenuation approximately for frequency range 300 to 400 Hz (i.e. = 300, = 400).

$x = \frac{f_2}{f_1}$ =*1.33*.

Number of octaves = $log_2(x) = \frac{log_{10}(x)}{log_{10}(2)}$

= 0.1239/0.3010 = 0.41.

16 db per 0.41 octave = 16/0.41 db per octave = 39.0 db per octave.

Low Pass Filter

From graph we have 18 db attenuation approximately for frequency range 2340 to 3000 Hz (i.e. = 2290, = 3000).

x = / = 1.31.

Number of octaves = $log_2(x) = \frac{log_{10}(x)}{log_{10}(2)}$

= 0.1173/0.3010 = 0.39.

18 db per 0.39 octave = 18/0.39 db per octave = 46.0 db per octave.

The stop band attenuation slope for both High Pass and Low Pass Filters is high meaning the Band Pass Filter is of high standard. The attenuation slope for the Low pass Filter is about 18% higher for the Low Pass Filter compared to that for the High Pass Filter.

Appendix 3: Alternative Airborne Electronics System Clock Pulse Generator

At the time of the March 1962 flight test of the Flight Memory System which, although there was full recovery of recorded signals, it was believed further work on some improvements may have been warranted. One of those that the author had noted was the possible derivation of the two inherent clock-style signals from a common reference. The two such clock-style signals are the 24 Hz Flight Data sampling rate and the 3500 Hz sine-wave amplitude modulator carrier frequency (Fig. 7). Of these signals, the 24 Hz is the more important and should be set as close as practical.

The lowest number divisible by 24 and 3500 is 21000. For a 21000 Hz reference signal a division by 875 (3x5x5x5x7) is required to provide a 24 Hz signal and is certainly feasible. For the 3500 Hz signal a division by 6 is required. The simplest approach would be to build a 21000 Hz rectangular wave oscillator, perform the frequency division and perform a rectangular to sine wave conversion at the output end.

An alternative reproduced from the author's 1961 notes is shown in Fig. A3. It comprises a 3456 Hz sinusoidal reference signal oscillator followed by a sine to square wave converter. The two divide-by-12 counter components provides the requisite 24 Hz output required for the Multiplexer and the Pulse Duration Modulator. The use of 3456 Hz in lieu of 3500 Hz for the Sine-wave Amplitude Modulator would be tolerable. It represents about 1% difference which could be taken care of by a slight variation in calibration values.

Appendix 4: Analog Output Offset Producer Calculations

The primary purpose of the Offset Producer was to provide an input to the Pulse Duration Modulator (PDM) that would produce a defined pulse-duration output from the Modulator when zero voltage output from the Multiplexer (Fig. 7) occurs. The Offset Producer is shown within a dash-rectangle as this function can be performed within the PDM. The circuit to perform this function external to the PDM comprises only three resistors. A secondary requirement was to ensure the input to the PDM was compatible with the overvoltage clipper in the PDM. The nominal clipper voltage is 5.8 V and the analogue voltage input must be clear of that. The duration of that pulse has to be accurately set to 10% of the output that would apply for full scale 5.0 V (100%) input from the Multiplexer. The Multiplexer transfers the transducer outputs (which, it was assumed, had low output impedance) to the Offset Producer. There is a "zero offset" adjustment in the PDM and if that were used the Offset Producer could have been used just to meet the secondary requirement noted above.

The Analog Output Offset Producer (Fig. A4) has two sections. The one on the left is a general network arrangement with each arm of a parallel arrangement containing an emf source and a resistance or conductance in series. If R is the resistance in ohm then conductance $G = 1/R$ mho. The output voltage e_c for the general network is given by:

$$e_c = \frac{e_1 G_1 + e_2 G_2 + \ldots + e_n G_n}{G_1 + G_2 + \ldots + G_n}$$

The use of "e" for emf (electromotive force), although its measurement unit is volt, is preferred here as we are considering electrical power sources usually derived from non-electrical sources (e.g. pressure in the case of a pressure transducer, chemical energy in the case of a battery etc.). The emf voltage for each "e_n plus G_n" arm is the open-circuit voltage (zero current) that could be measured across the arm. A further advantage of the use of this powerful network analysis is that two or more legs can be replaced with a single leg. For example, the first two legs can be combined as:

$$e_{12} = \frac{e_1 G_1 + e_2 G_2}{G_1 + G_2}$$

and the associated resistance is:

$$R_{12} = \frac{1}{G_1 + G_2} = \frac{R_1 R_2}{R_1 + R_2}$$

The general theory described above can be applied to other Flight Memory airborne and ground recovery circuits. It can now be applied to the practical circuit shown on the right in Fig. A4. In the first leg the Multiplexer output e_m is equivalent to e_1 in the first leg, + 24 V is equivalent to e_2 in the second leg, and e_3 is zero in the third leg.

For 100% transducer output, e_1 equals 5.0 V, and for $e_2 = 0$ define $e_c = k$. For e_1 equal to 0, the requirement (as indicated earlier) is for e_c to be equal to $k/10$. It is assumed that the output resistance of the multiplexer is low. The emf e_2 for the second leg is +24 V, one of the well-regulated DC supplies provided by the Airborne Power System. The required value of R_2 for a given value of R_1 can now be calculated:

$$G_1/G_2 = R_2/R_1 = (24\text{ V} / 5\text{ V}) \times 10 = 48$$

Next, we will check the value of e_c for $G_3 = 0$ (open circuit). Call it e_{12}.

$$e_{12} = (e_1G_1 + e_2(G_1 / 48)) / (G_1 + G_1 / 48)$$
$$= (48e_1 + e_2) /49$$

Substituting e_1 = 5V and e_2 = 24 V gives e_{12} = 5.39 V and the associated resistance is $R_1R_2/(R_1 + R_2)$ which equals $(48/49)R_1$.

Provided the R_2/R_1 relationship is maintained, the condition that the offset be equal to 10% of a full-scale transducer input will be maintained provided the value of R_1 is much greater than the output resistance of the signal source. If we nominate R_1 = 15 K, then R_2 will need to be 720 K. An adjustable trim resistor of 50K in series with a 680 K resistor could have been used for R_2.

There is no way of increasing the 100% transducer component in the network output without a pre or post-network non-inverting DC amplifier. Reducing it would be straight forward by a suitable selection of the R_3 resistance value.

To provide a 5.0 V (e_{co}) output for 100% transducer input plus the 0.5 V equivalent zero volt offset and a 10% sync over-voltage would require the R_3 value to be set to a calculated value that would produce a 5 V output for a 6 V input.

Define $R_{12} = R_1R_2/(R_1 + R_2)$:

$$e_{12}/e_o = (R_3 + R_{12}) / R_3 = 1 + R_{12}/R_3$$
$$R_3 = R_{12} / (e_{12}/e_{co} - 1) = R_{12}/((6.0/5.0) - 1) = R_{12} / 0.2$$
$$\text{For } R_1 = 15\text{ K}, R_{12} = 15(48/49) = 14.69\text{ K}$$
$$R_3 = 14.69/0.2 = 73.45\text{ K}$$

The above analysis can be simply applied for a different resistor R_1 value selection.

In practice, R_3 would probably comprise a fixed 68K resistor in series with an adjustable resistor (10K). If the zero-offset were performed in the Pulse Duration Modulator (PDM), the zero offset leg could be removed and the value of R_3 changed to provide a 5.0 V input to the PDM for a 5.5 V input to the Analog Output Offset Producer.

Appendix 5: Pulse Duration Modulator Trigger Delay Analysis

The Trigger Delay circuit (Fig. A5-A) is based on the use of Unijunction Transistor (UJT) 2N490 (Q_2). Some component labels used in the analysis herein differ from those used for the PDM in Fig. 19. Those shown in brackets in Fig. A5-A will be adopted for the analysis herein.

The unijunction transistor (UJT) is a three-lead silicon electronic semiconductor device with only one junction that acts exclusively as an electrically controlled switch. Transistor Q_1 also acts as a switch which is on when the Timer (Clock) input is high and off when it is low. The simplified equivalent circuit (Fig. A5-B) replaces Q_1 and associated components with switch SW, and the UJT is replaced with its standard equivalent circuit widely quoted in internet references. As indicated in the equivalent circuit the UJT has an emitter E and two base terminals B1 and B2. Internal base resistances R_{B1} and R_{B2} apply for the UJT. R_{B2} is shown as a variable and can take on a negative resistance value as inferred in the Characteristic Curve (Fig. A5-C). Negative resistance is a special property of the UJT where an increase in terminal voltage can result in a decrease in current.

Before proceeding with the analysis, the values of R_{B1} and R_{B2} (when positive resistance applies) need to be estimated. Define the following where η (Greek Alphabet lower case eta) denotes the Intrinsic Stand-off Ratio:

$$R_{BB} = R_{B1} + R_{B2}$$

$$\eta = R_{B1}/R_{BB}$$

Digitron Electronics (a supplier for the 2N490) gives typical values for the 2N490 are ($\eta = 0.56$) and ($R_{BB} = 7.6$ K). That gives typical values ($R_{B1} = 4.3$ K) and ($R_{B2} = 3.3$ K). At the time of writing the 2N490 was still commercially available.

Fig. A5-D provides a not-to-scale graphical representation of the relevant voltage versus time relationship for the trigger delay circuit. The UJT's emitter voltage V_E reveals a constant voltage portion followed by a curved portion the duration of which represents the trigger delay time t_D. For convenience, time t is defined to have a value of 0 at the start of a trigger delay as indicated in Fig. A5-D.

The constant voltage non-zero portion of the V_E graph corresponds to the ($t < 0$) portion of that graph when the Timer (Clock) is in the high state. The Timer (Clock) IN has been deliberately drawn as a non-square wave although the actual waveform may be a square wave. The wavelength is definitely 1/24 sec but the high-low composition is immaterial. For the constant voltage non-zero portion of the V_E graph, Q_1 (Fig. A5-A) is switched fully on, meaning switch SW (Fig. A5-B) is closed. When ($t < 0$) capacitor (C = 0.022 μF) is short-circuited. The use of approximate computed values is appropriate in this section.

At $(t = t_S)$ prior to ($t = 0$), the UJT's emitter E is subject to a step increase in V_E voltage (Fig. A5-D). Assuming zero emitter current for the UJT, emitter voltage V_E can be easily calculated.

$$V_{BB} = V_{CC} \frac{\frac{R_{BB}R_2}{R_{BB}+R_2}}{R_1 + \frac{R_{BB}R_2}{R_{BB}+R_2}}$$

$$= V_{CC} \frac{R_{BB}R_2}{R_{BB}R_1 + R_{BB}R_2 + R_1R_2}$$

$$V_E = kV_{BB} = kV_{CC} \frac{R_{BB}R_2}{R_{BB}R_1 + R_{BB}R_2 + R_1R_2}$$

Known parameter values can now be substituted to confirm, that the assumption that emitter current is zero, is valid:

$V_{CC} = 24$ V, $R_{BB} = 7.6$ K, $R_1 = 2.2$K, $R_2 = 10$ K

V_{BB} equals 15.9 V, voltage at right side of diode D (Fig. A5-D) is ηV_{BB} which equals 8.9 V, and the voltage V_E on the left side of diode D is 0 V for $(k = 0)$ and 8.9 V for $(k = 1)$. Since diode D requires a forward voltage dop of 0.7 V to allow current to pass, the assumption that emitter current will be zero for full range of *k* is confirmed.

At ($t = 0$) capacitor *C* has zero voltage across its terminals and it will receive a step in current equal to that flowing through R_2 before switch SW (Fig. A5-B) is opened. That current will reduce as *t* increases. The step in current can be represented by an equivalent step in the V_{CC} voltage (although. Emitter current will be zero initially, and if it remained at zero the voltage across capacitor *C* would rise to value $V_{CC}R_{BB}/(R_{BB} + R_1)$ when its steady state current was zero. However, an abrupt change occurs, prematurely, when emitter current starts to flow and R_{B1} exhibits negative resistance. The value of *t* when that occurs is the time delay.

Calculation of the time delay is not a simple matter and the author adopted the Laplace transform approach. The Laplace Transform *L* creates a function, call it *F(s)*, of frequency dependent parameters. The Laplace Transform simplifies the solution of differential equations and its general definition is:

$$L\{f(t)\} = F(s) = \int_0^\infty f(t)\, e^{-st} dt$$

The lower limit of integration is (t = 0) meaning f(t) = 0 for t < 0.

There are only two conversions of interest in this particular application where *L* and L^{-1} refer to Laplace Transform and Inverse Laplace Transform respectively:

$F(s) = L\{f(t)\}$	$f(t) = L^{-1}\{F(s)\}$
$\frac{1}{s}$	1
$\frac{1}{s - a}$	e^{at}

A very important relationship for two transforms *F(s)* and *G(s)* and any constants *a* and *b* is:

$$L^{-1}\{aF(s) + bG(s)\} = aL^{-1}F(s) + bL^{-1}G(s)$$

This means + or – and constants are directly transferrable between *s* and *t* domains.

Define $V_{BB}(s)$ as the voltage at the R_1–R_2–R_{BB} junction with respect to ground.

$$V_{BB}(s) = \frac{V_{CC}}{s} f(s) \text{ where } f(s) = \frac{Z}{R_1 + Z} \text{ and } z = \frac{R_{BB}\left(R_2 + \frac{1}{sC}\right)}{R_{BB} + R_2 + \frac{1}{sC}}$$

Expanding f(s) gives the following result:

$$f(s) = \frac{R_{BB}\left(R_2 + \frac{1}{sC}\right)}{(R_{BB}R_1 + R_{BB}R_2 + R_1R_2) + (R_1 + R_{BB})/sC}$$

$$= \frac{\frac{sR_{BB}\left(R_2 + \frac{1}{sC}\right)}{R_{BB}R_1 + R_{BB}R_2 + R_1R_2}}{s + \frac{1}{RC}} \quad where\ R = \frac{R_{BB}R_1 + R_{BB}R_2 + R_1R_2}{R_1 + R_{BB}}$$

$$= \frac{\frac{sR_{BB}\left(R_2 + \frac{1}{sC}\right)}{R(R_1 + R_{BB})}}{s + \frac{1}{RC}}$$

$$V_E(s) = V_{BB}\,\frac{kR_2 + \frac{1}{sC}}{R_2 + \frac{1}{sC}}$$

$$= \frac{V_{CC}}{s}\,\frac{\frac{sR_{BB}\left(R_2 + \frac{1}{sC}\right)}{R(R_1 + R_{BB})}}{s + \frac{1}{RC}}\,\frac{kR_2 + \frac{1}{sC}}{R_2 + \frac{1}{sC}}$$

$$= \frac{V_{CC}}{s}\,\frac{\frac{sR_{BB}\left(kR_2 + \frac{1}{sC}\right)}{R(R_1 + R_{BB})}}{s + \frac{1}{RC}}$$

$$= \frac{V_{CC}}{s}\,\frac{\frac{sR_{BB}\left(kR_2 + \frac{1}{sC}\right)}{R(R_1 + R_{BB})}}{s + \frac{1}{RC}}$$

$$= \frac{V_{CC}}{s}\,\frac{\frac{R_{BB}}{R_1 + R_{BB}} * \frac{kR_2}{R} * \left(s + \frac{1}{kR_2C}\right)}{s + \frac{1}{RC}}$$

$$= \frac{V_{CC}}{s} * \frac{R_{BB}}{R_1 + R_{BB}} * \frac{kR_2}{R} * \frac{s + \frac{1}{kR_2C}}{s + \frac{1}{RC}}$$

The following analysis will manipulate the above product into the sum of separate items that will allow direct transfer from "*s*" to the "*t*" domain.

$$V_E(s) = V_{CC}\left[\left\{\frac{R_{BB}}{R_1 + R_{BB}} * \frac{kR_2}{R} * \left(1 + \frac{R}{kR_2}\right)\right\}\frac{1}{s} - \frac{R_{BB}}{R_1 + R_{BB}}\,\frac{kR_2}{R}\left\{\frac{R}{kR_2} - \frac{s + \frac{1}{kR_2C}}{s + \frac{1}{RC}}\,\frac{1}{s}\right\}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R} * \left(1+\frac{R}{kR_2}\right)\right\}\frac{1}{s} - \frac{R_{BB}kR_2}{(R_1+R_{BB})R}\left\{\frac{R}{kR_2} - \frac{s+\frac{1}{kR_2C}}{s+\frac{1}{RC}}\frac{1}{s}\right\}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R}\right\}\frac{1}{s} + \frac{R_{BB}kR_2}{(R_1+R_{BB})R}\left\{\frac{R}{kR_2} - \frac{R}{kR_2} + \frac{s+\frac{1}{kR_2C}}{s+\frac{1}{RC}}\frac{1}{s}\right\}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R}\right\}\frac{1}{s} + \frac{R_{BB}}{R_1+R_{BB}}\left\{1 - 1 + \frac{kR_2}{R}\left(\frac{s+\frac{1}{kR_2C}}{s+\frac{1}{RC}}\right)\right\}\frac{1}{s}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R}\right\}\frac{1}{s} + \frac{R_{BB}}{R_1+R_{BB}}\left\{1 - 1 + \frac{kR_2}{R}\left(\frac{s+\frac{1}{kR_2C}}{s+\frac{1}{RC}}\right)\right\}\frac{1}{s}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R}\right\}\frac{1}{s} + \frac{R_{BB}}{R_1+R_{BB}}\left\{1 - \frac{s+\frac{1}{RC} - \frac{s}{R} - \frac{1}{RC}}{s+\frac{1}{RC}}\right\}\frac{1}{s}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R}\right\}\frac{1}{s} + \frac{R_{BB}}{R_1+R_{BB}}\left\{1 - \frac{s-\frac{kR_2s}{R}}{s+\frac{1}{RC}}\right\}\frac{1}{s}\right]$$

$$= V_{CC}\left[\left\{\frac{R_{BB}kR_2}{(R_1+R_{BB})R}\right\}\frac{1}{s} + \frac{R_{BB}}{R_1+R_{BB}}\left\{\frac{1}{s} - \frac{1-\frac{kR_2}{R}}{s+\frac{1}{RC}}\right\}\right]$$

Consider the expressions on the left and right sides of the + sign:

That on the left represents the value of the V_E voltage step at ($t = 0$). As indicated earlier the V_E step was used to simulate the step in the current through capacitor C at ($t = 0$). In reality there is no step in V_{CC} or V_E voltages at ($t = 0$). The step in V_E will be equal to its value just before ($t = 0$). The value of this expression has no effect on the trigger delay.

The expression on the right side of the + sign will be used in calculating the trigger delay. Define the part of V_E on the right of the + sign as V_{ED}.

$$V_{ED}(t) = V_{CC}\left\{\frac{R_{BB}}{R_1+R_{BB}}\left\{1 - \left(1 - \frac{kR_2}{R}\right)e^{-\frac{t}{RC}}\right\}\right\}$$

The instant when emitter current starts to flow for the unijunction transistor will represent the end of the trigger delay. Define t_D as the trigger delay. Conduction of silicon diode D in the equivalent circuit (Fig. A5-B) will occur when its forward voltage drop V_D is nominally 0.7 V. $V_{BB}(t)$ equals the value of $V_{ED}(t)$ when k equals 1.

$$V_{BB}(t) = V_{CC}\left\{\frac{R_{BB}}{R_1+R_{BB}}\left\{1-\left(1-\frac{R_2}{R}\right)e^{-\frac{t}{RC}}\right\}\right\}$$

$$V_{ED}(t) - \eta V_{BB}(t) = V_D$$

$$V_{CC}\left\{\frac{R_{BB}}{R_1+R_{BB}}\left\{1-\left(1-\frac{kR_2}{R}\right)e^{-\frac{t_D}{RC}}\right\}\right\} - \eta V_{CC}\left\{\frac{R_{BB}}{R_1+R_{BB}}\left\{1-\left(1-\frac{R_2}{R}\right)e^{-\frac{t_D}{RC}}\right\}\right\} = V_D$$

$$\left\{1-\left(1-\frac{kR_2}{R}\right)e^{-\frac{t_D}{RC}}\right\} - \eta\left\{1-\left(1-\frac{R_2}{R}\right)e^{-\frac{t_D}{RC}}\right\} = \frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}$$

$$1-\eta-\left\{1-\eta+\frac{R_2}{R}(\eta-k)\right\}e^{-\frac{t_D}{RC}} = \frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}$$

$$1-\eta-\left\{1-\eta+\frac{R_2}{R}(\eta-k)\right\}e^{-\frac{t_D}{RC}} = \frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}$$

$$e^{-\frac{t_D}{RC}} = \frac{1-\eta-\frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}}{1-\eta+\frac{R_2}{R}(\eta-k)}$$

$$e^{\frac{t_D}{RC}} = \frac{1-\eta+\frac{R_2}{R}(\eta-k)}{1-\eta-\frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}}$$

Define $h = \dfrac{1-\eta+\frac{R_2}{R}(\eta-k)}{1-\eta-\frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}}$

Let h_M be the value of h which correspons to the maximum delay t_{DM}.

$$h_M = \frac{1-\eta+\frac{\eta R_2}{R}}{1-\eta-\frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}}$$

$$t_{DM} = RC\ ln(h_M)$$

Using $R_1 = 2.2$ K, $R_2 = 10$ K, $R_{BB} = 7.6$ K, $R = 11.70$ K, $\eta = 0.56$, $C = 0.022$ µF,

$RC = 257$µs gives $h_M = 2.27$

$$ln(h_M) = \frac{log_{10}(h_M)}{log_{10}(h_M)} = \frac{0.3566}{0.4343} = 0.8210$$

$t_{DM} = 257 * 0.8210$ µs $= 211$ µs

For $(h = 1)$, $(t_D = 0)$ and the corresponding value of k can be determined.

$$1-\eta+\frac{R_2}{R}(\eta-k) = 1-\eta-\frac{V_D}{V_{CC}}\ \frac{R_1+R_{BB}}{R_{BB}}$$

$$k = \eta + \frac{V_D}{V_{CC}} \frac{R}{R_2} \frac{R_1 + R_{BB}}{R_{BB}} = 0.604$$

Hence, only about 60% of the R_2 next to capacitor C provides adjustable t_D in range (0 to 211 μs).

Perhaps a 5 K potentiometer in series with a 4.7 K or 5.1 K resistor (E24 or lower range standard resistor values) would be a more appropriate replacement for R_2. If the voltage drop across diode D is ignored $(i.e.\ V_D = 0)$, then $(k = \eta = 0.56)$ is a reasonable approximation.

When emitter current begins to flow the UJT's R_{B1} switches from positive to negative resistance and the UJT abruptly switches on causing V_E also to abruptly switch to or close to 0 V. That state will be maintained as the current through capacitor *C* drops to zero and while the TIMER (CLOCK) IN signal remains low. The negative going leading edge of the V_E signal produces a trigger signal for the PDM's bistable flip flop via the 300 μμF capacitive coupling.

Appendix 6: Analysis of Effect of Using Pulsed Sine-wave Flight Data Modulation

1. Preview

The purpose of this Appendix is to provide an explanation for the presence of a regular undefined amplitude audio signal that could be heard at the ground station recovery stage when no voice signal was present on the recorded audio channel. This signal will be referred to herein as the "spurious signal" At the time when the Flight Memory system was being tested and its future application (if any) was unknown, the need to resolve this technical problem was considered to be significant. The only thing that the author remembers as being crystal clear is that the spurious signal sounded like the song of a cricket insect (only males sing). Its strength relative to 100% audio level and its waveform versus time is unknown, either because no measurements were made, or if they were, no records were kept.

It transpired that the Flight Memory system never went into commercial production although it was the first device to be developed that resembled the modern "Black Box". It was instrumental in the development of the Red Egg magnetic wire aircraft accident data recorder produced (1965 - 1980) by the British company S. Davall & Sons Ltd in Middlesex, England.

The analysis here of the problem is far from simple and comprises:

- A "Fourier Analysis" which provides a theoretical prediction of spurious signal generation.
- An estimate of the significance of the spurious audio signal.
- Review of observed audio characteristics of the spurious signal.
- How to minimise the spurious signal if deemed necessary.

2. Fourier Analysis

The Fourier Analysis is an extension of an analysis (Ref. 13 p3) by the author in support of the design of the filter for the Ground System recovery of the flight data.

The Flight Data signal input to the Combiner has the form of a sinusoidal voltage burst of varying duration at a rate of 24 Hz. A Fourier analysis of a single burst (Fig. A6) will be considered here. Initially, the analysis will consider the number of sine-wave cycles in the burst as a variable. Later, a specific value of 10 cycles as shown in Fig. A6 will be used.

Consider a sinusoidal pulse train defined by $f_1(t) = sin\,\omega_0 t$ in the range $-\frac{T}{2} < t < \frac{T}{2}$ and being zero elsewhere (Fig. A6). Let n = number of cycles of the sine-wave occurring in time T, then:

$$f_0 = \frac{\omega_0}{2\pi} = \frac{n}{T}$$

where f is frequency measured in hertz (Hz) or cycles per second and ω is angular frequency measured in radians per second. Lower-case symbol f is used for both "frequency" and "function" parameters herein but when used for the latter it will be followed by brackets.

Since we are considering a single burst of sine waves (as distinct from a repetitive burst) in the present instance, the Fourier Series presentation is not applicable and the Fourier Integral presentation is required.

The Fourier Integral is defined as:

$$F_1(\omega) = \int_{-\infty}^{\infty} f(t)\, e^{-j\omega t}\, dt \tag{1}$$

and the corresponding time function is given by:

$$f_1(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F_1(\omega)\, e^{j\omega t}\, d\omega \tag{2}$$

The pair of equations (1) and (2) is usually referred to as a "Fourier Transform Pair". $F_1(\omega)$ may be expressed as:

$$F_1(\omega) = a(\omega) - jb(\omega) \tag{3}$$

Expanding equation (1) gives:

$$F_1(\omega) = \int_{-\infty}^{\infty} f_1(t)\, (\cos \omega t - j\, sin\, \omega t)\, dt$$

For the special case under consideration $f_1(-t) = -f_1(t)$ and hence $f_1(t)$ is an odd function.

For $f_1(t)$ odd:

$$F_1(\omega) = -2j \int_0^{\infty} f_1(t) \sin \omega t\, dt \tag{4}$$

Substituting $f_1(t) = \sin \omega_0 t$ $\left(\text{up to time } t = \frac{T}{2}\right)$ gives:

$$F_1(\omega) = -2j \int_0^{\frac{T}{2}} \sin \omega_0 t \sin \omega t\, dt$$

$$= -2j \int_0^{\frac{T}{2}} [\cos (\omega_0 - \omega)t - \cos (\omega_0 + \omega)t\,]\, dt$$

$$= -j \left[\frac{\sin (\omega_0 - \omega)}{\omega_0 - \omega}\frac{T}{2} - \frac{\sin (\omega_0 + \omega)}{\omega_0 + \omega}\frac{T}{2}\right]$$

Comparing with equation (3) it follows that:

$$a(\omega) = 0$$

$$b(\omega) = \frac{\sin (\omega_0 - \omega)}{\omega_0 - \omega}\frac{T}{2} - \frac{\sin (\omega_0 + \omega)}{\omega_0 + \omega}\frac{T}{2} \tag{5}$$

Expanding equation (2) it follows that:

$$f_1(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} -jb(\omega)\, (\cos \omega t + j \sin \omega t)\, d\omega$$

For $f_1(t)$ real $Im\, f_1(t)$ must be zero which will be so since $b(\omega)$ is odd. Hence:

$$f_1(t) = \frac{1}{\pi}\int_0^{\infty} b(\omega) \sin \omega t\, d\omega \tag{6}$$

From (6) it can be seen that $f_1(t)$ may be considered as an infinite sum of infinitesimal components $b(\omega)\Delta\omega \sin \omega t$ where $\Delta\omega$ is a small increment in ω. We cannot talk here in terms of discrete frequency components as the contribution to $f_1(t)$ at any particular frequency is

infinitesimal. However, we can say that the contribution to $f_1(t)$ by components in the band between $\omega_1 \; and \; \omega_2$ is given by:

$$f_1(t) = \frac{1}{\pi}\int_{\omega_2}^{\omega_1} b(\omega) \sin \omega t \; d\omega \qquad \text{which is finite.}$$

If b(ω) is relatively high in any specific frequency band, then it can be concluded that this frequency band contributes significantly to $f_1(t)$, whereas if b(ω) is relatively small in some other frequency band, then it can be concluded that the contribution to $f_1(t)$from this band is small.

Returning .to equation (5) and substituting $T = \frac{2\pi n}{\omega_0}$ we obtain:

$$b(\omega) = \frac{1}{\omega_0}\left[\frac{\sin \pi n \left(1 - \frac{\omega}{\omega_0}\right)}{1 - \frac{\omega}{\omega_0}} - \frac{\sin \pi n \left(1 + \frac{\omega}{\omega_0}\right)}{1 + \frac{\omega}{\omega_0}}\right] \tag{7}$$

If it is assumed that *n* is an integer or, in other words, that an integral number of cycles is considered, then when $\omega = \omega_0$

$$b(\omega_0) = \frac{\pi n}{\omega_0} = \frac{n}{2f_0} \tag{8}$$

$$\text{since lim as } \left(1 - \frac{\omega}{\omega_0}\right) \to 0 \text{ of } \frac{\sin \pi n \left(1 - \frac{\omega}{\omega_0}\right)}{1 - \frac{\omega}{\omega_0}} \text{ equals } \pi n.$$

For $\omega = \frac{k}{n}$ where k is an integer not equal to n, $b(\omega) = 0$ and hence nodes occur.

$$b(\omega) = -\frac{1}{\omega_0}\left[\frac{\sin \pi n \frac{\omega}{\omega_0}}{1 + \frac{\omega}{\omega_0}} + \frac{\sin \pi n \frac{\omega}{\omega_0}}{1 - \frac{\omega}{\omega_0}}\right]$$

$$= -\frac{\sin \pi n \frac{\omega}{\omega_0}}{\omega_0} \times \frac{2}{1 - \left(\frac{\omega}{\omega_0}\right)^2}$$

If the above equation is normalized by dividing by $b(\omega_0)$ as derived above in equation (8) the following results:

$$\frac{b(\omega)}{b(\omega_0)} = -\frac{\sin \pi n \frac{\omega}{\omega_0}}{\mathrm{n}\pi} \times \frac{2}{1 - \left(\frac{\omega}{\omega_0}\right)^2} \tag{9}$$

When $\omega = \omega_0$, $\left|\frac{b(\omega)}{b(\omega_0)}\right|$ is obviously equal to 1. Checking that the RHS of equation (9) also has value 1 (or -1) presents added difficulty.

$$\frac{b(\omega)}{b(\omega_0)} = -\frac{\sin \pi n \frac{\omega}{\omega_0}}{\mathrm{n}\pi \left(1 - \frac{\omega}{\omega_0}\right)} \times \frac{2}{1 + \frac{\omega}{\omega_0}}$$

Using $(\omega = \omega_0 - \Delta\omega_0)$

$$\left[lim\ as\ \Delta\omega_0\ \rightarrow 0\ of\ \frac{sin\ \pi n\left(1-\frac{\Delta\omega_0}{\omega_0}\right)}{\pi n\frac{\Delta\omega_0}{\omega_0}}\right]\left[lim\ as\ \Delta\omega_0 \rightarrow 0\ of\ \frac{sin\ \pi n\left(-\frac{\Delta\omega_0}{\omega_0}\right)}{\pi n\frac{\Delta\omega_0}{\omega_0}}\right] = -1$$

since adding any integer number of π does not change the sine value.

Consider the special case for (*n = 10)* which corresponds to the length of the shortest sine-wave burst for the Flight memory system.

$$\frac{b(\omega)}{b(\omega_0)} = -\frac{\sin 10\pi\frac{\omega}{\omega_0}}{5\pi\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]} \tag{10}$$

In Fig. A7 $\left|\frac{b(f)}{b(f_0)}\right|$ $\left(\text{which is equal to } \left|\frac{b(\omega)}{b(\omega_0)}\right|\right)$ has been plotted as a function of $\frac{f}{f_0}$ $\left(\text{which is equal to } \frac{\omega}{\omega_0}\right)$.

The 3 db half-power limits for the Flight Memory audio filter have been indicated in Fig. A7. Contributions within the audio pass-band from the Flight Data signal are evident even though those close to ($f = f_0$) are dominant.

For longer sine-wave bursts, node separation will be smaller (it will vary inversely as the number of sine-wave cycles in the burst).

3. Estimate of the Significance of the Spurious Audio Signal

Producing an accurate estimation of the level of the spurious signal would be very difficult and is not warranted. In an idealised but unreal world the audio filter would provide infinite rejection of signals outside the audio passband. A reasonable approximation would be to consider the spurious audio signal to be comprised of just two elements:

1. The part of the 3500 Hz signal burst that is transferred to the audio filter passband.
2. The part of the 3500 Hz signal burst that is passed by the audio filter on data recovery.
3. Conclusion

Item 1 estimation:

The sharp sine-wave burst amplitude transitions at the leading and trailing ends of the burst are responsible for spurious components being transferred to the cockpit voice band at the Combiner stage prior to recording. The Fourier Integral analysis above did not include what happens after (n = 10) cycles of the 3500 Hz sinewave burst. The post trailing edge response is considered in detail in Appendix 8.3. In effect, the contribution of the trailing edge is effectively equivalent to the leading edge response but delayed by the duration of the sinewave burst.

While Fig. A7 indicates the unfiltered frequency spectrum for the first 10 cycles of a Flight Data signal burst, the absolute contributions for all other sinewave bursts would be the same since only leading and trailing burst transitions result in transfers to the audio filter passband. The proportion P_{10} of the first 10-cycles of the burst transferred to the audio passband, will now be estimated.

From the above Fourier Integral analysis, the following approximation applies:

$$P_{10} = \frac{A_1}{A_2}$$

where A_1 equals the area of Fig.A7 half-sine lobes in passband and A_2 equals total lobe area.

The area of a lobe is proportional to height by width and the result is:

$$P_{10} = 0.25 = 25\%$$

That implies that, without any filtering, the sound intensity of that transferred to the audio passband was approximately equal to that for 2.5 cycle of the 3500 Hz signal.

The proportion P_n reduces as n is increased as illustrated in the following table, where the amplitude of the 3500 Hz Flight Data signal is assumed to be equal to the 100% audio signal value.

% Flight Data duration	0	50	100	110 (Sync)
n	10	60	110	120
P_n	25%	4.2%	2.3%	2.1%

Item 2 estimation:

The extraction of the audio signal from the composite Cockpit Voice and Flight Data signal was performed during data recovery using the Ground Station Unit (GSU). That extraction process used an identical filter to that applied to limit the audio passband to 400 Hz to 2400 Hz prior to recording.

From Fig. 14 it is estimated that the residual 3500 Hz component passed by the audio filter is about –33 db (2.2%) relative to the mid-band audio filter value. The author holds no details of the relative amplitude of the 3500 Hz signal passed to the Combiner (it is adjustable (Fig. 23) over a wide range. A reasonable assumption would be that it would have been set equal to 100% audio level.

Item 3 conclusion

- There is a short duration spurious signal transferred to the audio passband for each Flight Data sample. That intensity corresponds to that for 2.5 cycle of the 3500 Hz signal.
- The audio filter will pass about 2.2% of the 3500 Hz signal assuming 100% 3500 Hz signal amplitude equals 100% audio signal value. A filter with higher 3500 Hz signal reduction could have improved the level of rejection.
- The spurious signal is a combination of the *Item 1* and *Item 2* contributions. If the leading and trailing edge contributions are added, then the impact of *Item 1* is about double that of *Item 2* at 100% 3500 Hz pulse duration.
- There was no recording made in 1961/2 of the spurious signal level. It is concluded that it was low enough to have no significant effect on audio signal intelligibility.

3. Review of Observed Audio Characteristics

The frequency analysis of a single sine-wave burst in the previous section provides negligible help in defining what sound the listener hears. All that can be concluded is that some short

duration sound snippets within the pass-band of the audio filter will be present 24 times per second.

The author's impression was that, under test conditions with no microphone sound, the spurious sound was similar to that emanating from a cricket insect at his home at the time in Hawthorn a suburb of Melbourne, Victoria, Australia.

After investigating what cricket insects were common in Australia it became clear that two types, Field and Mole crickets, dominate. The fundamental frequency of the Mole cricket song is about 2 kHz while that for the Field cricket is much higher (in the vicinity of 8 kHz). That means the Field cricket song is well outside the Cockpit Voice filter passband and no further consideration of its song is warranted.

Although it is difficult for the author to relate the song he heard in 1961 to recorded songs available on the internet, the author believes the Mole cricket song (Ref. A2) recorded in Surrey Hills (a suburb in Melbourne, Australia close to where the author lived in 1961) is the closest match. There is no discernible chirp like the more conventional, about 4.5 Hz, noted for a Brisbane Mole cricket (Ref. A3). Brisbane is about 1700 km north of Melbourne and its climate is very different to that for Melbourne and that could have a significant influence on the cricket's song characteristics. The Surrey Hills cricket song was examined using Audacity software and a burst rate of about 75 Hz was revealed. The level of the spurious signal was low enough to tolerate for the flight test and there was a need to complete the test so that other "more important work" could proceed. It transpired that no further design or investigative work was done after the 1962 flight test.

It is possible that the 75 Hz burst rate was a genuine chirp rate although the author was unable to locate any reference to support such a value.

According to Ref. A4 the Mole Cricket rubs its wings at the rate of 90 cycles per second. Any spurious signal for the Flight Memory system would have been likely to have occurred at the leading and trailing edges of the sinewave bursts (i.e. twice the 24 Hz sampling rate). Although the 48 Hz signal would have the leading edge components regularly occurring time-wise, some irregularity would be present for the trailing edge components. The 48 Hz signal is about 2/3 of the frequency (75 Hz) noted for the Surrey Hills cricket. Those figures are close enough to support a proposition that the spurious sound heard by the author when replaying recorded signals with no microphone input would be likely to be similar to the song of the Surrey Hills Mole cricket.

Thea author concluded that the referenced Surrey Hills Mole Cricket song, which did not contain a low frequency chirp, appears to be atypical for the species although a higher frequency wing-rubbing could be a possible cause.

4. How to Minimise Spurious Signal if Deemed Necessary

The following define options that could have been considered if further development work would have been undertaken after the 1962 flight test. Minimising the problem would have been straight forward once its cause was established.

Since the problem was not so severe that cockpit voice intelligibility was significantly impaired a "do nothing" approach would have been a valid option.

A high pass filter could have been inserted between the Sine-Wave Amplitude Modulator and the Combiner (Fig. 7) to reduce the component transferred to the audio filter passband. A 3 db cut-off frequency of about 3000 Hz may have been appropriate but the actual value would need to have been adjusted experimentally. Alternatively, a band-pass filter could have been used.

The residual 3500 Hz component passed by the Ground Station filter could have reduced by changing the filter to one with higher rejection in the vicinity of 3500 Hz.

Appendix 7: Decision that Had Major Impact on Power System Development

During the development of the Mk 2 Flight Memory System, special group meetings of pertinent ARL staff were held to review progress and formalise decisions relevant to the project. Each meeting had the title “Inter-Divisional Meeting for discussion of the Crash Recorder Project”. The meetings were chaired by the Chief Superintendent (Sir Lawrence Coombes) and other attendees normally comprised Superintendents and project development staff from participating Divisions (Mechanical Engineering and Aerodynamics). At the first meeting the Chief Superintendent appointed the author as Minute-taker. Meetings were held in 1961 on 22-March, 11-May, 20-June, 27-June and 14 September, and in 1962 on 22-May and 16-October. Minutes were prepared after each meeting. The Minutes were included with a wide range of other documents (Ref. A5) in the National Archives held in the National Library Canberra. Other copies of what was sent to the National Library are held by the Warren family and the author.

A mostly-readable copy of the Minutes of the second meeting held on the 11-May-1961 follows. At that meeting it was decided that an emergency battery would be included in the airborne system to allow recording to continue if an electrical power failure occurred during flight. That decision had a major impact on the Airborne Power System development as the simplest solution was to derive both normal and power-loss-emergency power from DC sources. The chosen setup was to derive normal power from the aircraft 28 VDC supply and the emergency power from a rechargeable 24 VDC battery supply. The other standard aircraft supply (200 VAC inter-phase 400 Hz) would have provided a simpler implementation if no emergency battery had been required. The relevant decision from the meeting has been highlighted in red a copy of the minutes which follows on the next two pages.

Inter - Divisional Meeting For Discussion of Crash Recorder Project

Minutes of the meeting held at 2.30 PM. Thursday, the 11th May, 1961, in the office of the Superintendent of Aerodynamics, Administrative Building.

Present.	ARL	L.P. Coombes	(Chief Superintendent)
		T.S. Keeble	(Supt. Mech. Eng. Division)
		H.M. Nelson	(A/Supt. Aerodynamics Division)
		G.P. Rundle	
		D.R. Warren	
		K.F. Fraser	
		W.E. Boswell	
Visitor.		V.B. Mursell	(Supervising Engineer Telecommunications Branch)
Apologies.		J.N. Lake	
		W.F.L. Sear	

GENERAL BUSINESS

REPORTS

1. Report to the Controller, Research & Development

An estimate of the expenditure (totalling £6,000) required for plant, materials and outside contracts in the development of the first working model of the A.R.L. Crash Recorder was sent to the Controller.

2. Present Position with Regard to Test Aircraft

DCA have agreed to make aircraft available for testing of the ARL Recorder and have appointed Mr. Frank Shanahan as liaison officer. With regard to any aircraft modification, which may be required, it has been made clear that the appropriate drawings must be submitted for approval before any alterations are made.

3. Report on Discussions with Ansett - ANA and the National Instrument Co.

Ansett - ANA expressed interest in the ARL Crash Recorder and would probably have been prepared to give assistance if the Recorder could have been produced in a fully engineered form by January, 1962. In any case they said they would be prepared to provide aircraft for the testing of the Recorder, during normal airline operations. National Instrument Co. were prepared to manufacture an engineered version of the Recorder or any individual components, if required, at a nominal charge.

4. Report of Technical Progress

Dr. Rundle gave the following report :-

(i) Assembly of the basic electronics unit is now in hand.

(ii) Work is proceeding in the design of the power supply.

(iii) The question of the best sampling switch to be purchased is still under consideration. Most commercially available commutation switches, are very expensive, and have a very short life. In the meantime other types of sequential sampling are being considered.

DISCUSSION

1. Power Supply

It was generally agreed that the power should be taken

.../2

directly off the 28 V. DC supply (not from the AC invertors). There was some discussion as to what type of motor would be best for the wire deck. An AC [illegible] motor had the advantage that no commutation was required, and hence such a motor would have longer life and would require less maintenance.

2. Discussion with RAAF

Mr. Coombes suggested that it would be a good idea if the RAAF were approached to see if they expressed any interest in the ARL Recorder, and if so whether they would be prepared to make aircraft available for testing of the Recorder. Mr Keeble undertook to approach the RAAF.

3. Switch

It was decided that a Sigma Instruments stepping motor type switch, costing roughly £50, be purchased forthwith.

4. Engineering Version of Recorder

Mr. Mursell said that when ARL had produced a satisfactory working model, he felt sure that some arrangement could be made to have it produced in a fully engineered form.

5. General Comments

Mr. Keeble said that it was essential that the Recorder be relatively cheap, especially if it is to have any impact in the military field. He also presented the possibility of the Recorder finding a market outside Australia. With regard to the wire spools themselves, he suggested that both a fireproofed version and a version suitable for ejection be made simultaneously.

The meeting closed at 4.00 PM.

K.F. Fraser

K.F. FRASER
SECRETARY

Next Meeting

The next meeting is to be arranged approximately 2 months hence, unless a requirement for a meeting before that date becomes apparent.

Appendix 8: Analysis of the Ground Station Flight Data Extraction Process

1. Preview

The sharp wavefront of the suddenly applied sinusoidal voltage, used in the recording system, would not be transmitted through the Flight Data Extractor's band-pass filter (even if the frequency of the excitation voltage were equal to the centre frequency of the filter) hut would experience initial attenuation. It is the purpose of this Appendix to relate the number of cycles, which occurred during the transition to full amplitude, to the bandwidth of the band-pass filter. The case of a filter having a maximally flat steady state amplitude response was considered, as such a filter has optimum rejection of signals in the adjacent cockpit voice band.

A complete analysis of the topic is provided in the author's Ref. 13. This Appendix will examine the main findings from that Reference that are relevant to this analysis.

2. Frequency Responses of Maximally Flat Band-Pass Filters

The frequency response of a maximally flat band pass filter (also known as a Butterworth filter) is considered in this Section. The following parameters are defined:

$\omega =$ angular frequency in radian/sec

$f =$ frequency in cycles per second ($f = 2\pi\omega$)

$\omega_0 =$ mid-band value of ω

$f_0 =$ mid-band value of f

$B(j\omega) =$ is the output of the filter at angular frequency ω. It is usually represented as a function with real and imaginary components ($j^2 = -1$).

$b =$ bandwidth [difference between upper and lower cut-off frequencies of $B(j\omega)$] where cut-off frequencies occur where $|B(j\omega)|$ is –3 db below mid-band value.

$b_R =$ bandwidth in radians per second

$b_F =$ bandwidth in Hz (cycles per second)

$n =$ number of poles in filter (see below for explanation)

About Poles and Zeros:

The author used pole terminology extensively in Ref. 13 when referring to Laplace and Z transformations. The *poles* and *zeros* of a transfer function are the frequencies for which the value of the denominator and the numerator of the transfer function becomes zero respectively. The values of the *poles* and the *zeros* of a system determine whether the system is stable, and how well it performs. More detailed information is available in Ref. A6.

The magnitude of $B(j\omega)$ as derived for Equation 35 in Ref. 13 is given as:

$$|B(j\omega)| = \frac{1}{\sqrt{\left[1+\left\{\frac{\omega_0}{b}\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)\right\}^{2n}\right]}} \text{ where } |B(j\omega)| \text{ is assigned the value of 1 } for\ (\omega = \omega_0).$$

A family of $\left(|B(j\omega)| \text{ versus } \frac{\omega}{\omega_0}\right)$ for $\left(\frac{b_R}{\omega_0} = 0.2\right)$ in each curve for $n\ in\ range$ $\{(n = 1)\ to\ (n = 4)\}$ is provided in Fig. A8.

The general results depicted in Fig. A8 can be compared with the particular case of the Flight Memory Ground Station flight data band-pass filter.

Using $\left(\frac{b_F}{f_0} = \frac{b_R}{\omega_0} = 0.2\right) and\ (f_0 = 3500\ Hz)$ gives filter bandwidth ($b_F = 700\ Hz$). That for the Ground Station was similar but slightly smaller at 600 Hz. A comparison of the attenuation rate with that of the Ground Station filter of Fig. 54 reveals the rate for the Ground Station filter lies closest to the (n = 2) curve.

3. Response of Band-Pass Filter to a Suddenly Applied Sinusoidal Voltage

The response of a band-pass filter to a finite burst of sine waves can be conveniently derived, using the principle of superposition, from the response of the filter to a sine-wave suddenly applied and maintained for infinite time.

The output $e_A(t)$from a unity amplitude sine wave excitation suddenly applied and maintained for infinite time is defined below.

$$e_A(t) = H(t)\sin(\omega_C t + \beta)$$

where $H(t)$ is the Heaviside Unit Step Function, ω_C is the angular frequency (radian per sec) of the sine-wave and β is the initial (t = 0) angle of the sine-wave.

The output $e_B(t)$from an identical sine-wave excitation suddenly applied at $(t = T)$ and maintained for infinite time is defined below.

$$e_B(t) = H(t - T)\sin(\omega_C t + \beta)$$

The output $e_1$from a burst of sine-waves of duration T is thus given by:

$$\begin{aligned} e_1(t) &= e_A(t) - e_B(t) \\ &= \{H(t) - H(t - T)\}\sin(\omega_C t + \beta) \end{aligned}$$

For a linear system the response of the band-pass filter to an excitation $e_1(t)$ is simply the response of the filter to $e_A(t)$ minus the response to $e_B(t)$. It follows from the above analysis that just $e_A(t)$ needs to be considered as, with its assessment, the response to the full sine-wave burst can be derived. The response of linear systems, such as the band-pass filter's voltage versus time output for a given voltage input versus time, is conveniently assessed using the Laplace transformation as an intermediate analysis. As indicated in Appendix 4, the Laplace Transform L simplifies the solution of differential equations and its general definition is:

$$L\{f(t)\} = F(s) = \int_0^\infty f(t)\, e^{-st} dt$$

The lower limit of integration is (t = 0) meaning $\{f(t) = 0\}$ for ($t < 0$) and 1 for ($t \geq 0$).

Let $E_1(s)$ be the Laplace transform of $e_A(t)$, $B(s)$ be the Laplace transform of the filter and $E_2(s)$ the Laplace transform of the output voltage.

$$e_A(t) = H(t)\ \sin(\omega_C t + \beta)$$

$$E_1(s) = L\{H(t)\ sin(\omega_C t + \beta)\}$$

$$E_2(s) = B(s)E_1(s)$$

Using the Ref. A7 Transform tables the following apply:

$$L\{H(t)\ sin(\omega_C t + \beta)\} = cos(\beta)\ L\{sin(\omega_C t)\} + sin(\beta)L\{cos\ (\omega_C t)\}$$

$$= \frac{\omega_C \cos(\beta)}{s^2 + {\omega_C}^2} + \frac{s \sin(\beta)}{s^2 + {\omega_C}^2}$$

$$= \frac{\omega_C \cos(\beta) + s \sin(\beta)}{s^2 + {\omega_C}^2}$$

$$E_2(s) = \frac{s \sin(\beta) + \omega_C \cos(\beta)}{s^2 + {\omega_C}^2} B(s)$$

For the following analysis, it will be assumed that the sine-wave burst starts from zero at $(t = 0)$ and hence $(\beta = 0)$. In that case:

$$E_2(s) = \frac{\omega_C}{s^2 + {\omega_C}^2} B(s)$$

$B(s)$ in the above general equation for $E_2(s)$ is an intricate function which varies with the number of poles n in the filter. A complete analysis is provided in Ref. 13.

4. Application of Narrow Band Approximation for Band-Pass Filter

The Flight Memory Ground Station Unit filter meets the narrow-band condition and that greatly simplifies the analysis. In that case ω_C can be considered to be mid-way between the $-3db$ bandwidth boundaries. The relationship between the amplitude of the response of the band-pass filter to the unit step response of a high-pass filter is provided in Ref. 13. In that Reference "low" instead of "high" was used and in that case the trailing edge of the sine-wave burst would apply.

	Excitation		Filter Transfer Function	Response	
	Time function	Laplace transform		Laplace transform	Time function
High-pass filter	*H(t)* (unit-step)	$\frac{1}{s}$	$P(s)$ bandwidth b	$\frac{P(s)}{s}$	$f_H(t)$
Band-pass filter	*H(t)* $e^{j\omega t}$	$\frac{1}{s - j\omega_0}$	$P(s - j\omega_0)$ bandwidth 2b	$\frac{P(s - j\omega_0)}{s - j\omega_0}$	$e^{j\omega t} f_H(t)$

Using Euler's formula gives: $\{e^{j\omega t} = cos(\omega t) + j\ sin\ (\omega t)\}$. Separating the $sin\ (\omega t)$ gives:

Band-pass filter input $= H(t) \sin(\omega_0 t)$

Band-pass filter output $= f_H(t)\ sin\ (\omega_0 t)$

Summarising this result, we can say that the amplitude of the response of a band-pass filter of centre frequency $\frac{\omega_0}{2\pi}$ and narrow bandwidth to a suddenly applied sinusoidal carrier, $H(t) \sin \omega_0 t$, is equal to the unit step response of the equivalent high pass filter having half the bandwidth of the band-pass filter. The responses of the high pass filter and the equivalent band-pass filter are illustrated in Fig. A10.

5. Unit Step Response for High Pass Filter

The purpose of this Section is to obtain the amplitude of the band-pass filter output. That means evaluating $f_H(t)$ which was defined in the previous Section. A full analysis is provided in the author's Ref. 13 Section 5.3. It provides results for range (n = 1) to (n = 4). The result for

($n = 2$) will be provided here as that value for n closely matches that applicable to the Flight Memory Flight Data Signal Extractor.

Let *a(t)* be the step time response of the high pass filter of bandwidth b, and let *A(s)* be its Laplace transform.

$$A(s) = \frac{P(s)}{s}$$

For n = 2:

$$A(s) = \frac{b^2}{s\left\{\left(s + \frac{b}{\sqrt{2}}\right)^2 + \left(\frac{b}{\sqrt{2}}\right)^2\right\}}$$

$$= \frac{1}{s} - \frac{\left(s + \frac{b}{\sqrt{2}}\right) + \frac{b}{\sqrt{2}}}{\left(s + \frac{b}{\sqrt{2}}\right)^2 + \left(\frac{b}{\sqrt{2}}\right)^2}$$

$$a(t) = 1 - e^{-\frac{b}{\sqrt{2}}t}\left(\cos\frac{b}{\sqrt{2}}t + sin\frac{b}{\sqrt{2}}t\right)$$

$$= 1 - \sqrt{2}\, e^{-\frac{b}{\sqrt{2}}t} sin\left(\frac{\pi}{4} + \frac{b}{\sqrt{2}}t\right)$$

since $\left(sin\frac{\pi}{4} = cos\frac{\pi}{4} = \frac{1}{\sqrt{2}}\right)$.

Put the bandwidth of the bandpass filter equal to $k\omega_0$.

$$b = \frac{k\omega_0}{2}$$

The $a(t)$ time responses as functions of $k\omega_0$, for the range $\{(n = 1)\ to\ (n = 4)\}$, have been plotted in Fig. A11 (which is a copy of Figure 11 in Ref. 13).

6. Comparison of the Band-Pass Filter Time Response for a Rectangular Input with that for a Sine-Wave Burst Input

The analyses of the previous Sections have considered the Flight Data band-pass filter as if it were receiving the pre-recorded sine-wave bursts from the Airborne Flight Memory System. Bandwidth limits imposed by the recording and playback processes would mean some filtering would occur before the signal is received at the input to the Ground Station Flight Memory band-pass filter. The idealized overall Flight Memory Flight Data filtering process is illustrated in Fig. A11 which has four graphs:

(a) Rectangular input gate for 3500 Hz sine-wave burst.
(b) Thirteen-cycle burst of 3500 Hz sine-wave.
(c) Narrow band filter time response for rectangular input.
(d) Narrow band filter time response for rectangular sine-wave burst input.

Items (a) and (b) relate mainly to the recording phase. Items (c) and (d) relate mainly to the recovery phase.

Appendix 9: Simultaneous Multiple-Channel-Analogue Output Selection Circuit

The Fig. A12 circuit is a copy of that provided by the author in Ref. 12 (Figure 24). It was the author's theoretical design that was never built and tested.

For simultaneous analogue decoding of all channels, the channel selector of Fig. 75 could have been replaced with a diode matrix associated with the binary outputs T11 to T16 of the Binary Counter (Sec. 5.2.3.2.2.2). Gate signals would appear successively at the various outputs of the diode matrix and analogue voltages associated with the corresponding ramp voltages would be formed across the charging capacitors in a similar manner to that described for the single analogue circuit of Fig. 76.

At the time of the 1962 Flight Memory validation flight the only low-speed chart recorder available was a Speedomax model (manufactured by Leeds and Northrup). While the author has no record of the model number, it was known that it was a single-channel-only pen recorder. From that perspective, since no multi-channel recorder was available, simultaneous presentation of signals was not an available option.

Even if a multi-channel pen chart reorder were available, implementation issues would have arisen. To avoid pen cross-over, vertical separation limiting range or horizontal (time offset) separation would have been required.

With the single-channel-at-a-time requirement, great care would need to be taken to make sure recording start-times for each channel were the same.

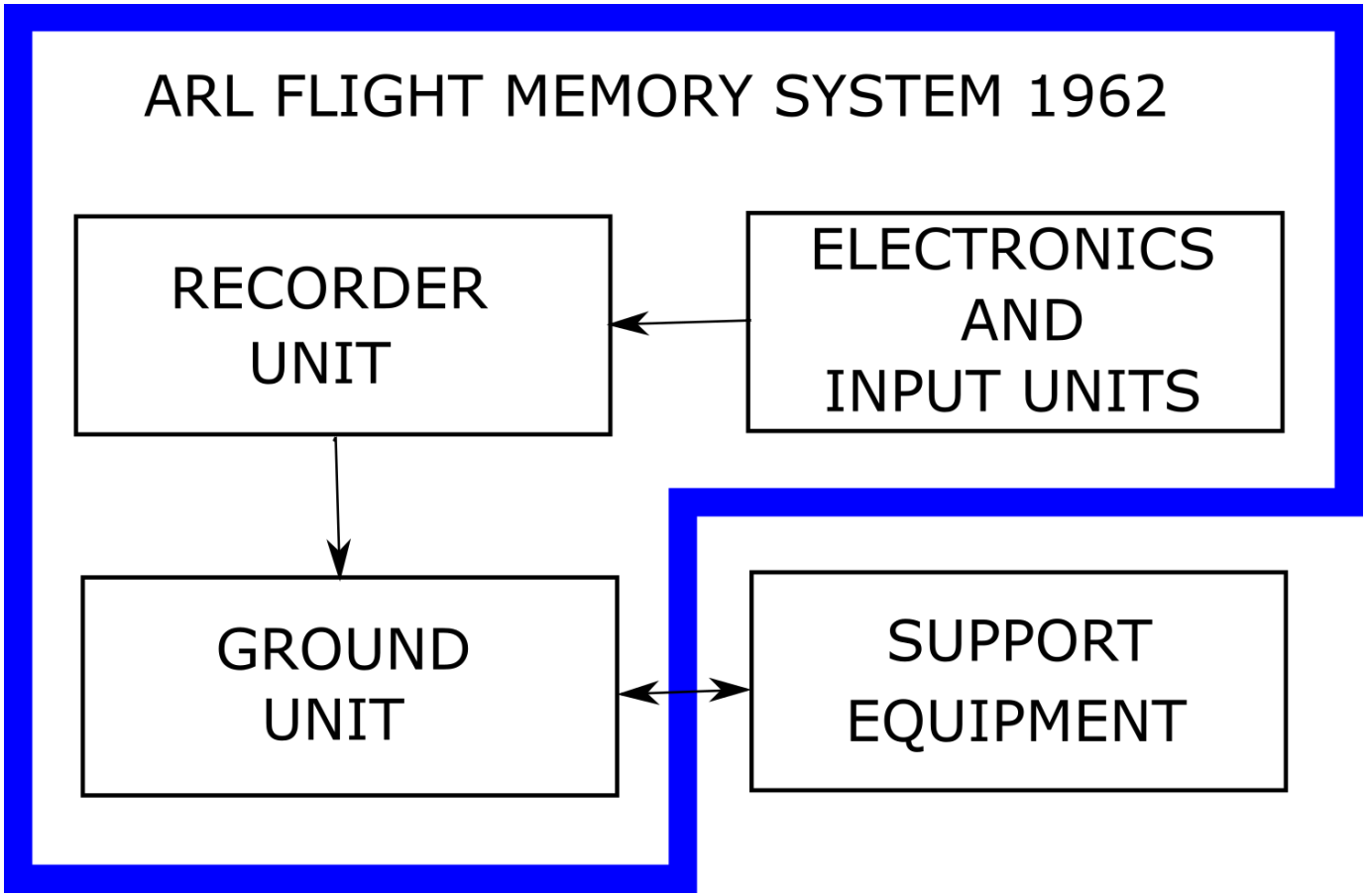
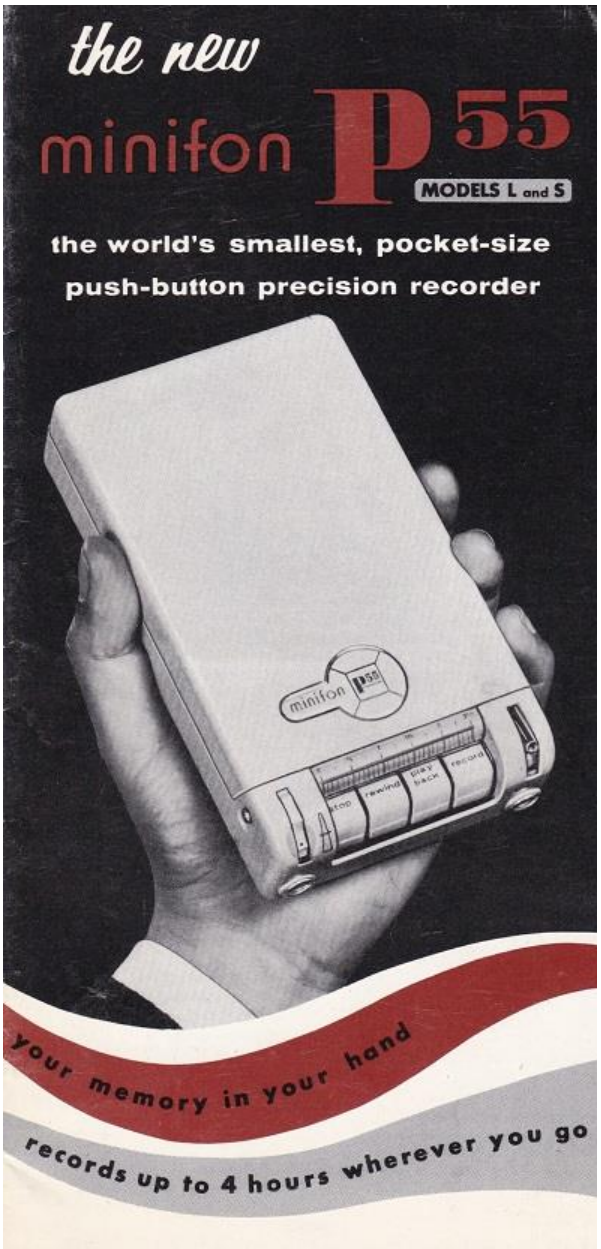


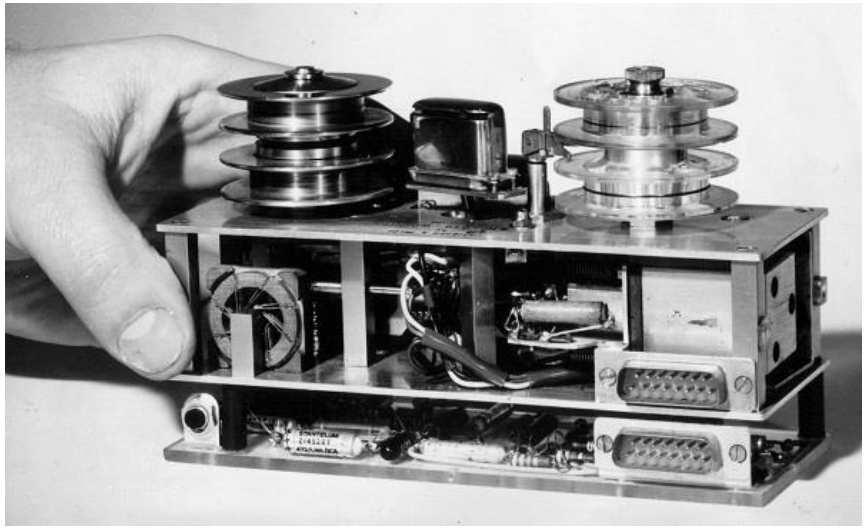
Figure 1: Simplified ARL Flight Memory System 1962



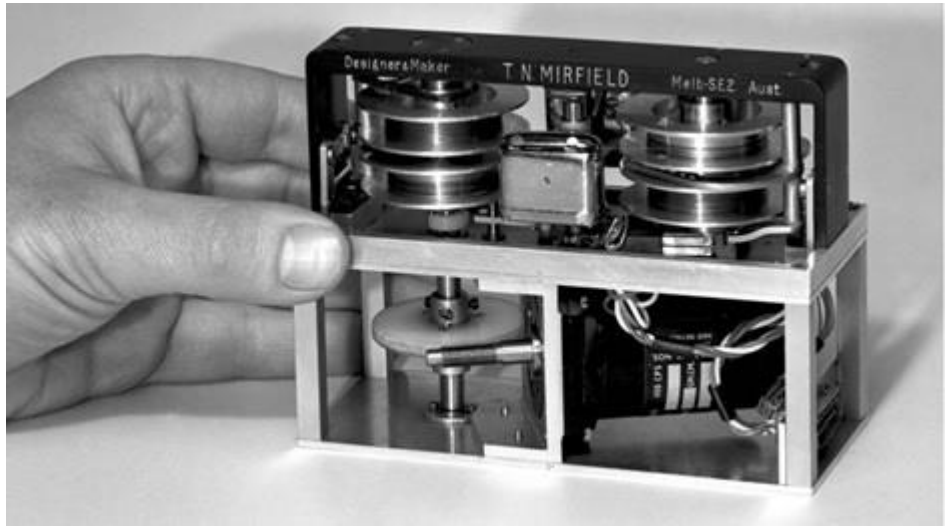
Recorder

Specification

Figure 2: Minifon P55 Wire Recorder



Mk 1 Recorder (1958)



Mk 2 Recorder (1962)

Figure 3: Flight Memory System Recorders

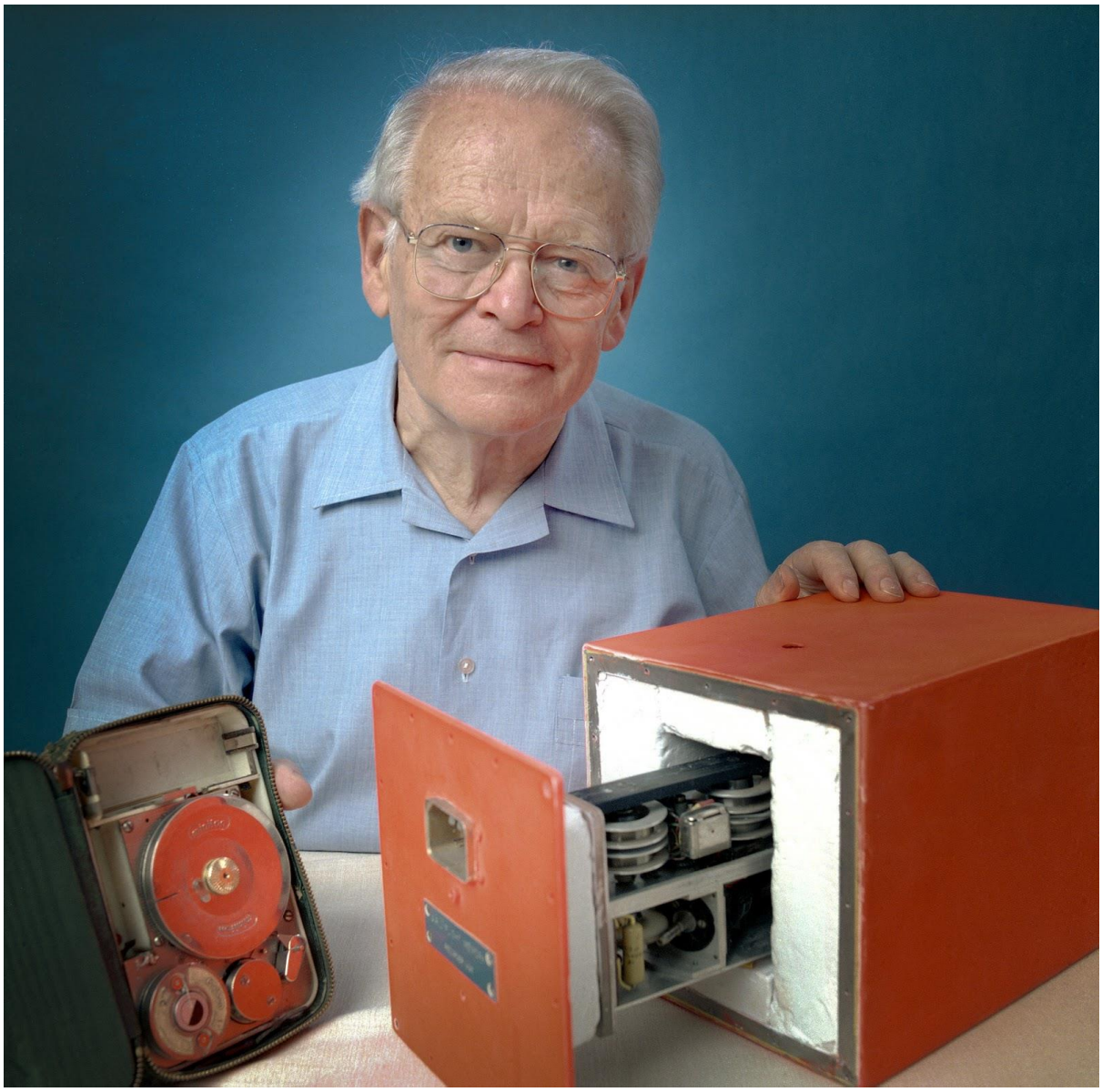


Figure 4: Mk 2 Recorder Partially in Case (with Dr Warren and Minifon Recorder)

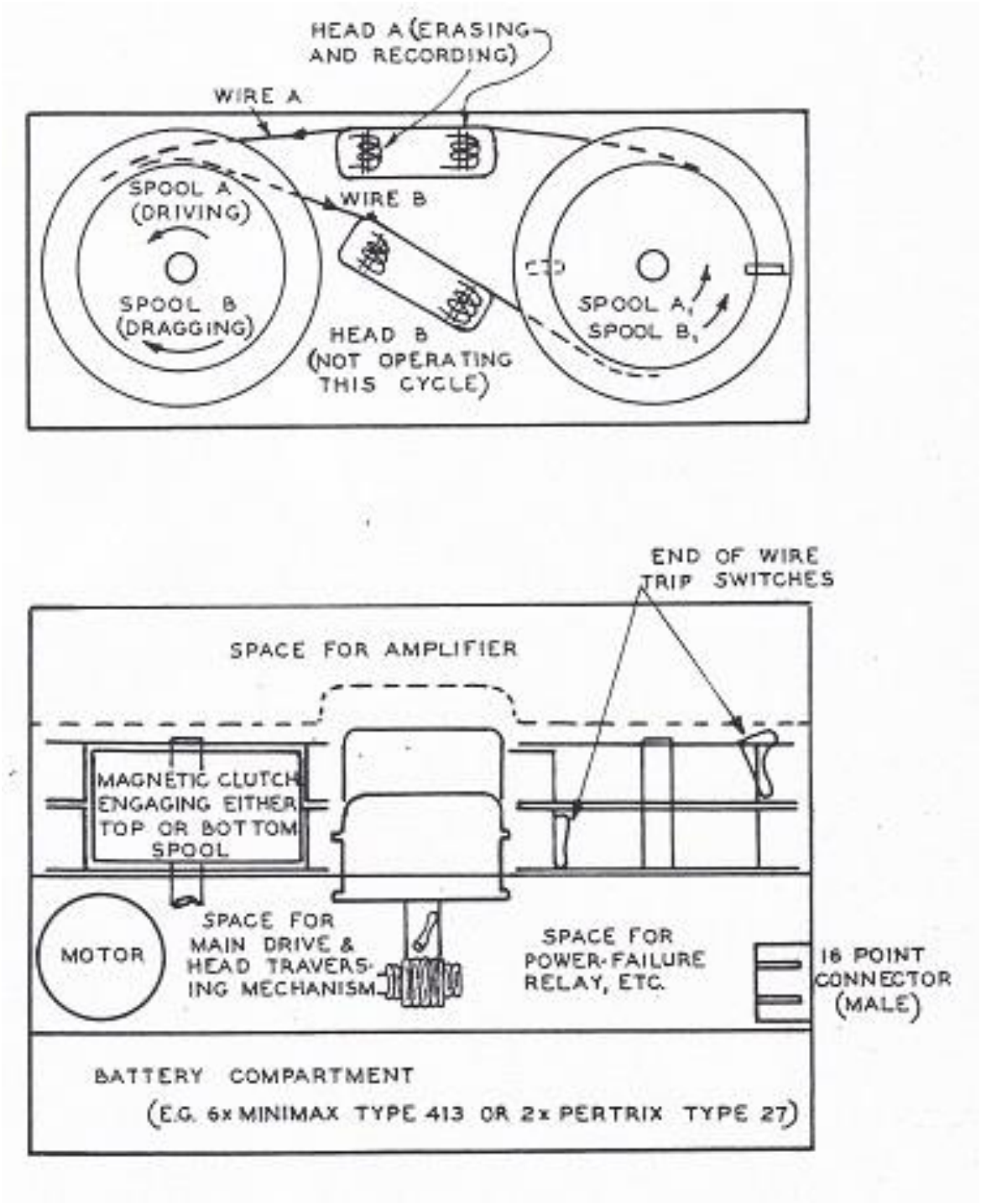


Figure 5: Recorder Memory Mechanism

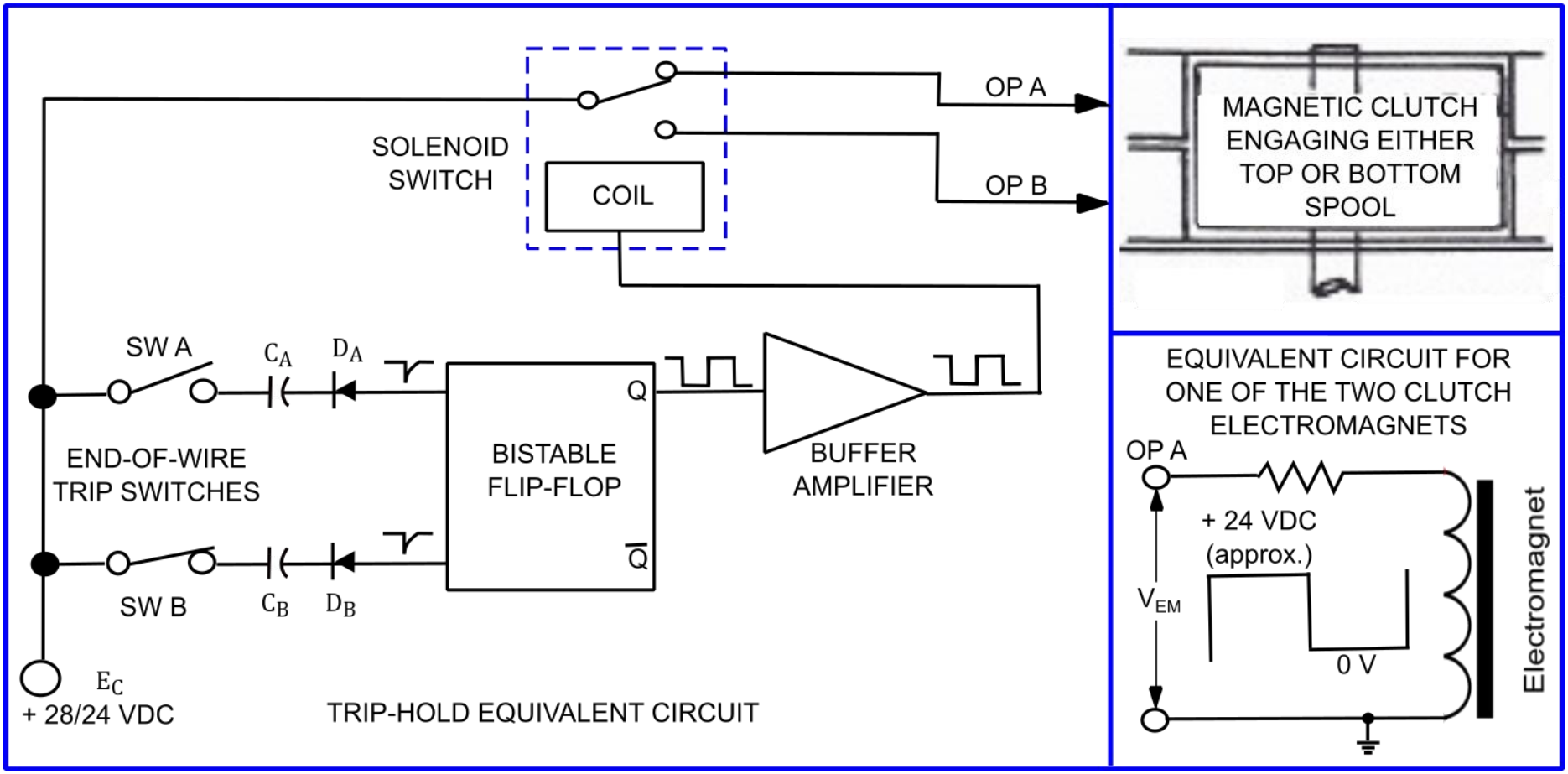


Figure 6: Recorder Simplified Equivalent Electrical Circuit

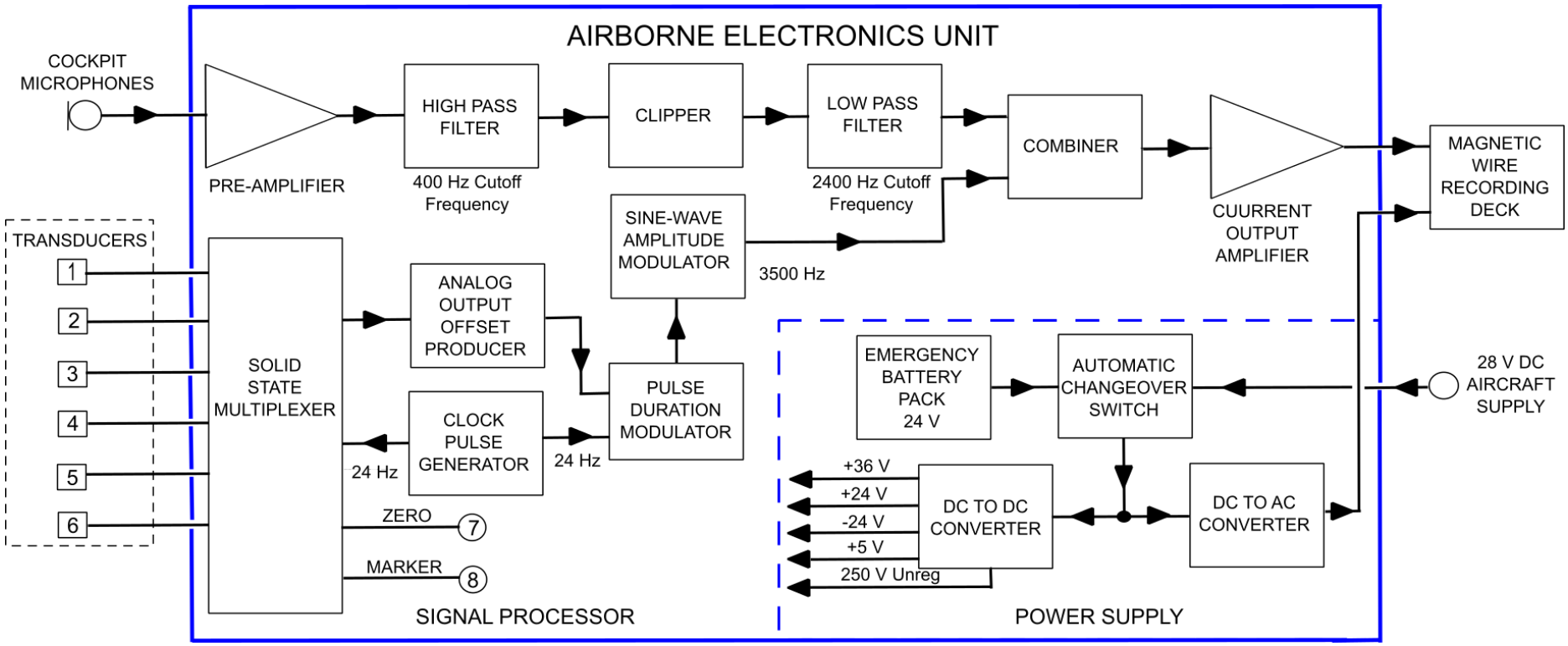


Figure 7: Airborne Flight Memory System Block Schema

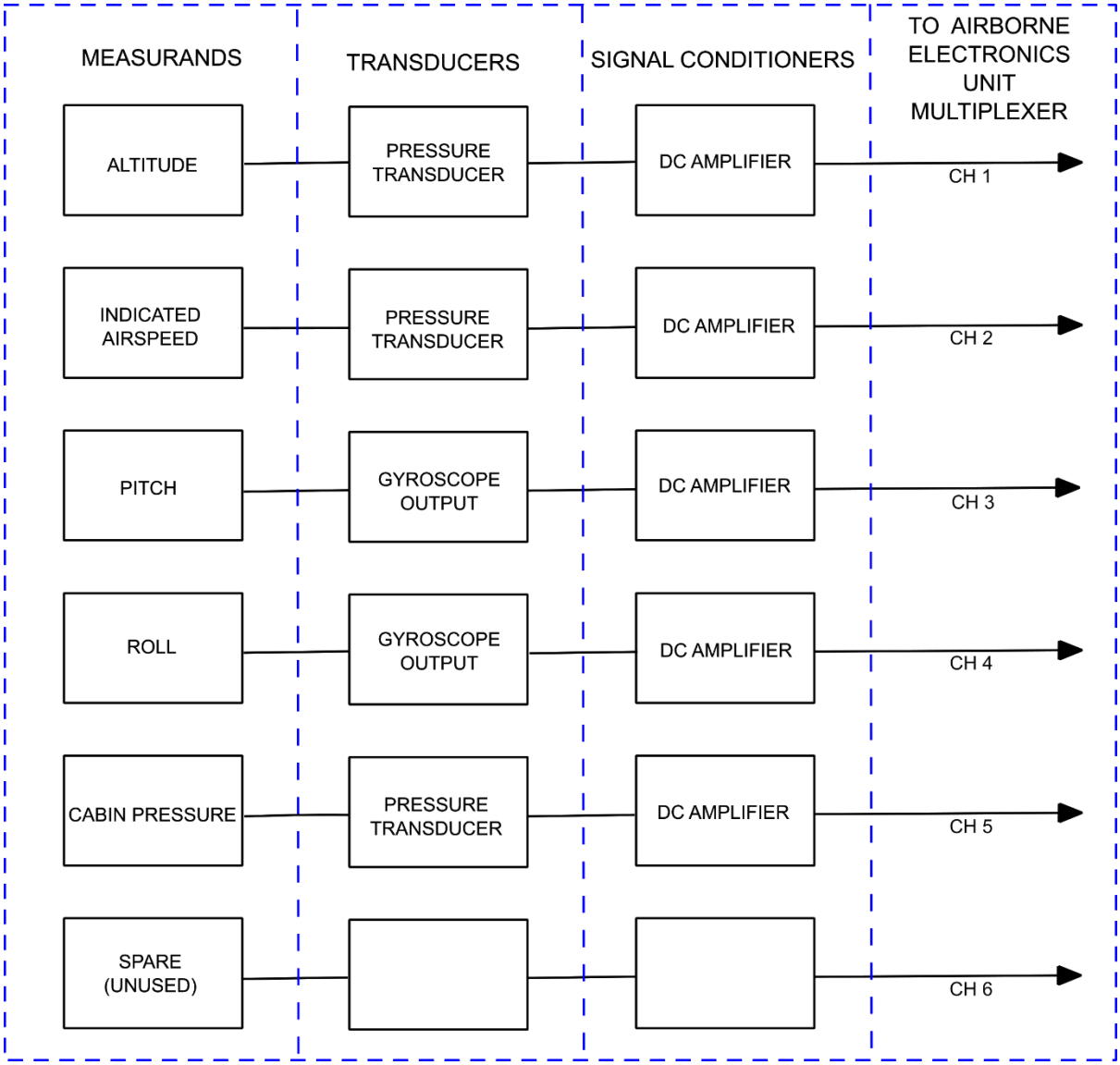


Figure 8: Aircraft Transducer Arrangement for 1962 Flight Memory Test Flight

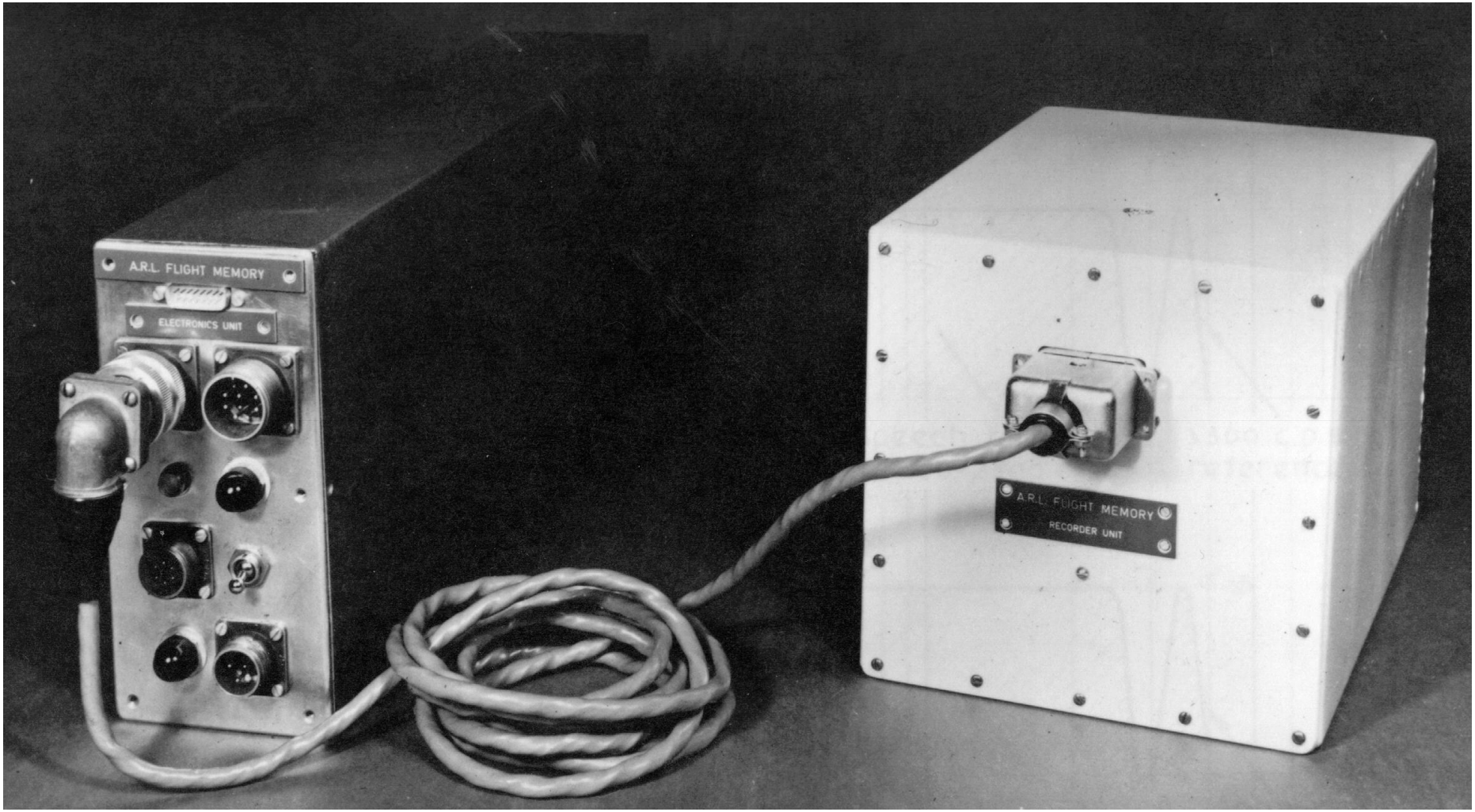


Figure 9: Electronics Unit in Case Beside Recorder

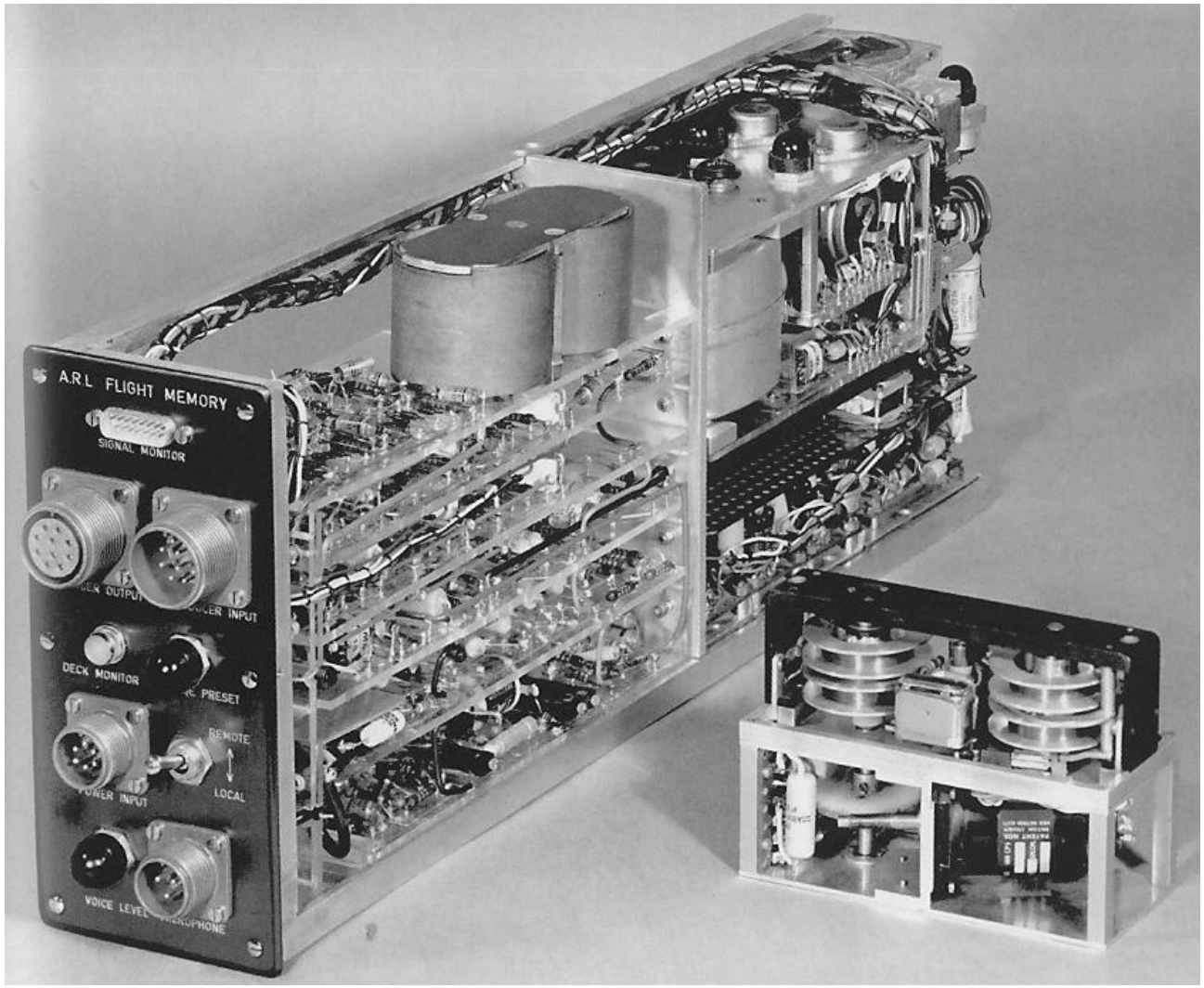


Figure 10: Electronics Unit Out of Case beside Recorder

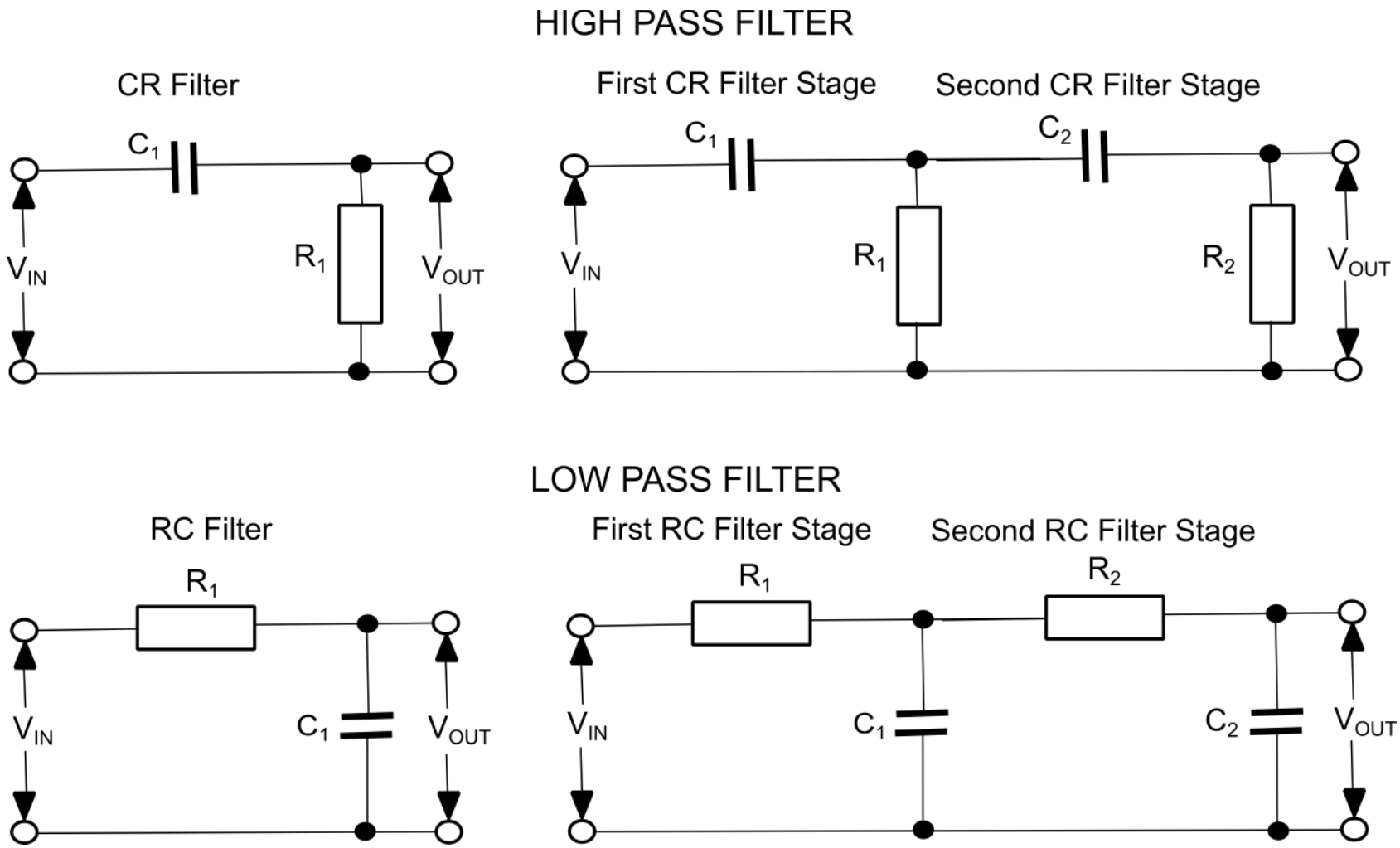


Figure 11: Basic Filters Using R (Resistor) and C (Capacitor) Components

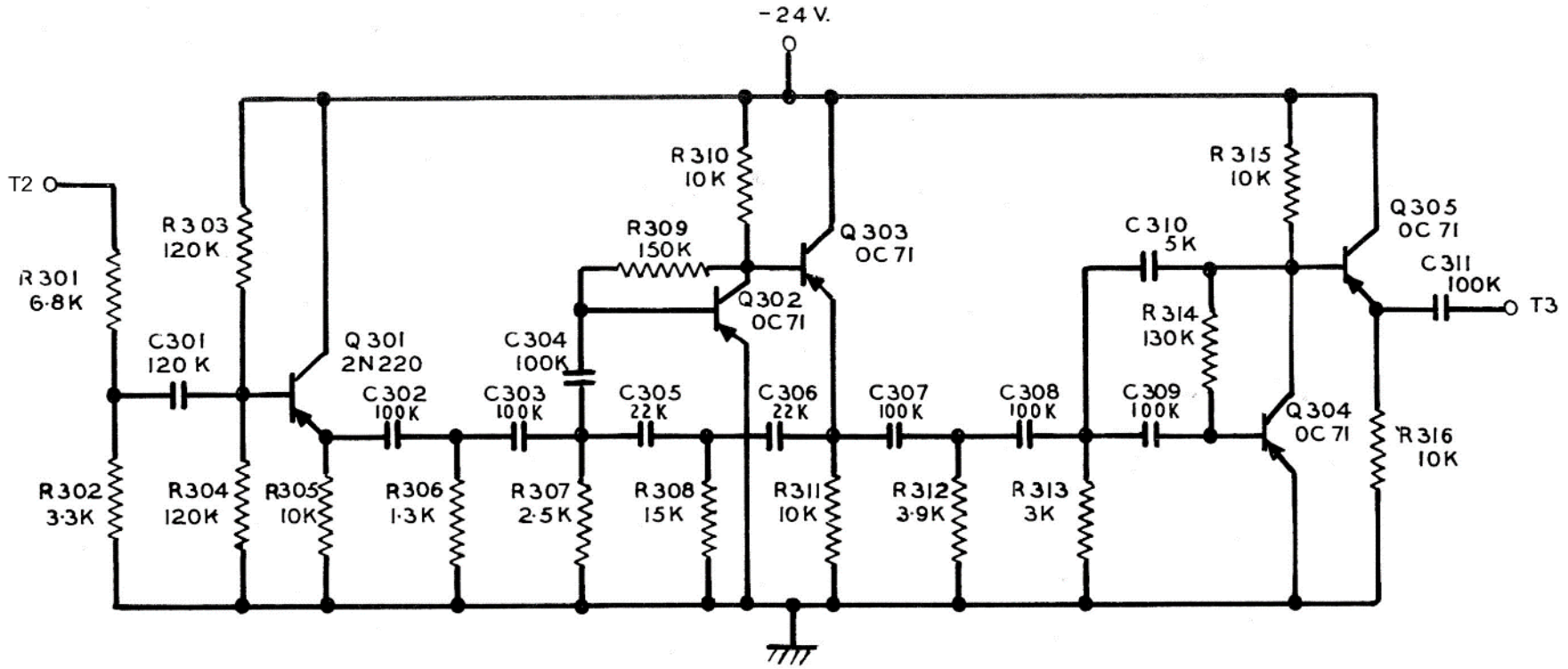


Figure 12: Cockpit Voice High Pass Filter

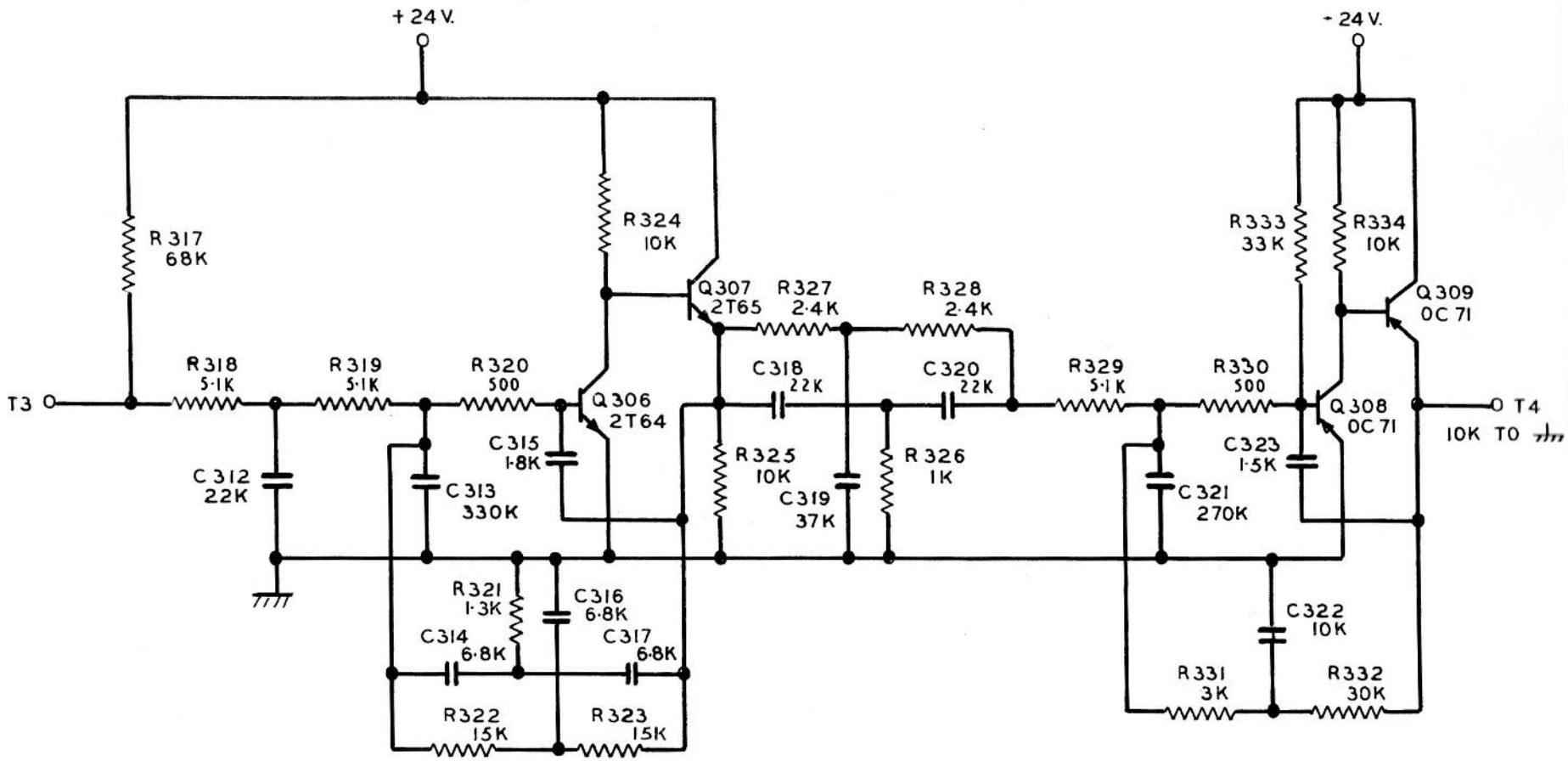


Figure 13: Cockpit Voice Low Pass Filter

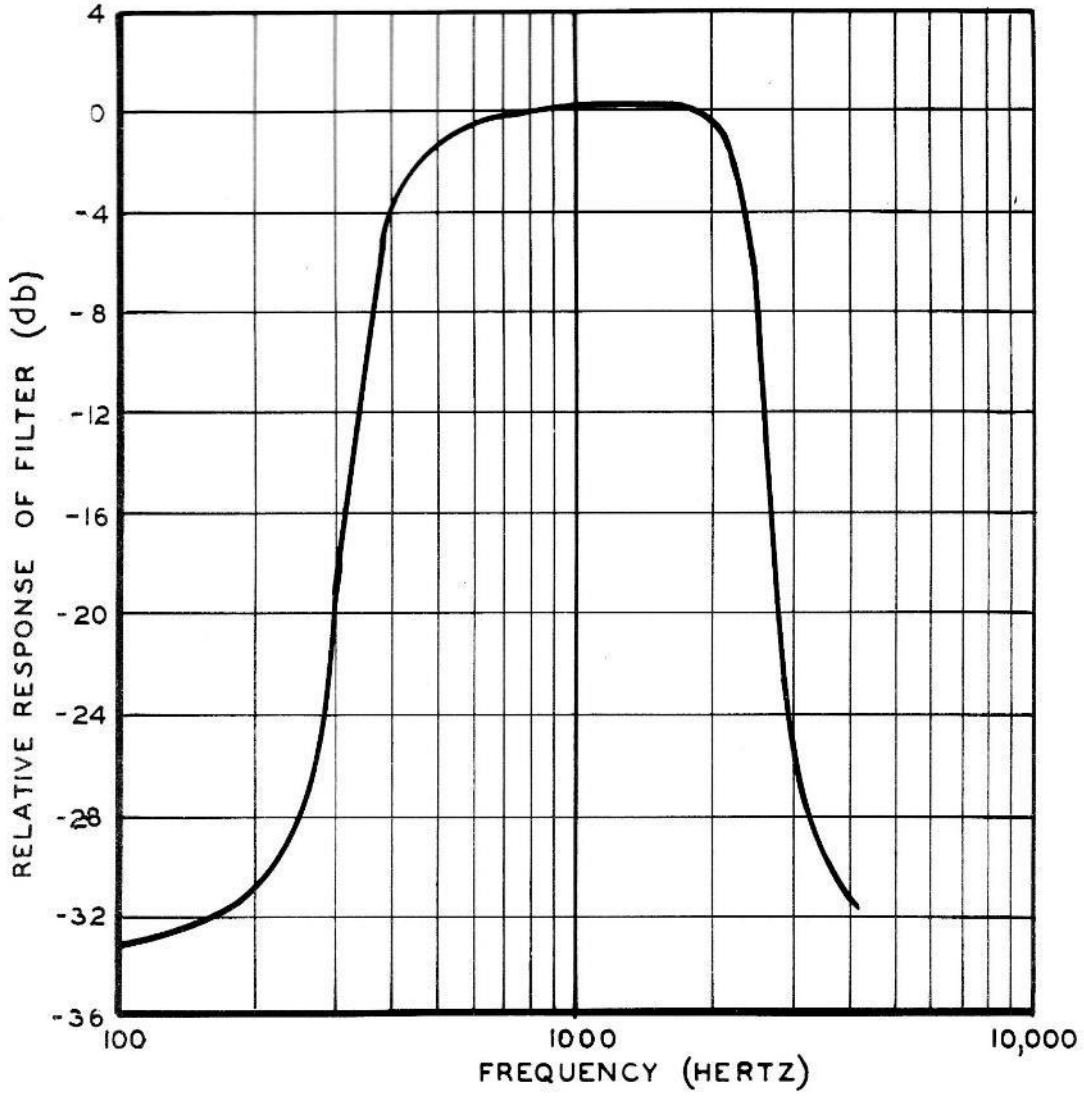


Figure 14: Cockpit Voice Band Pass Filter Frequency Response

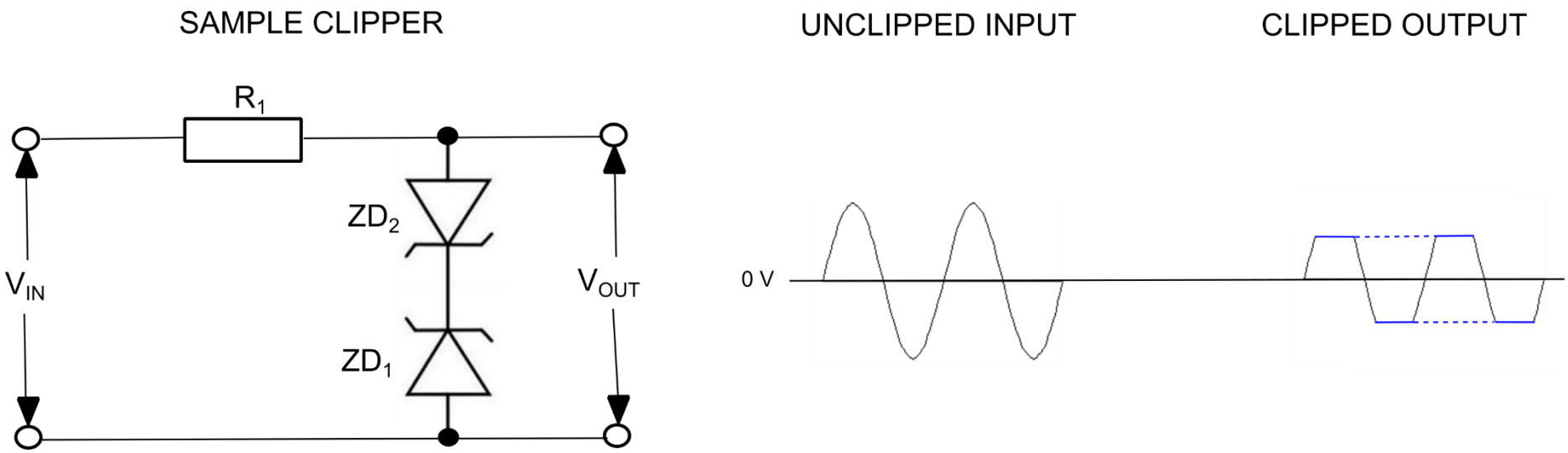


Figure 15: Cockpit Voice Signal Sample Clipper

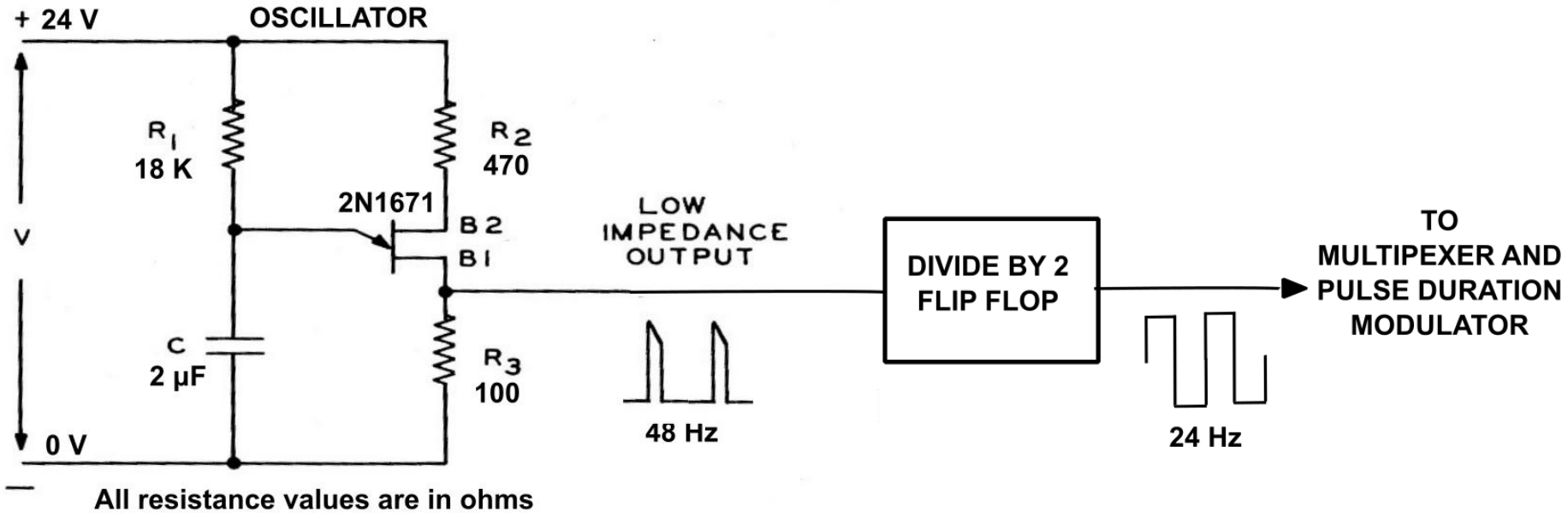


Figure 16: Clock Pulse Generator

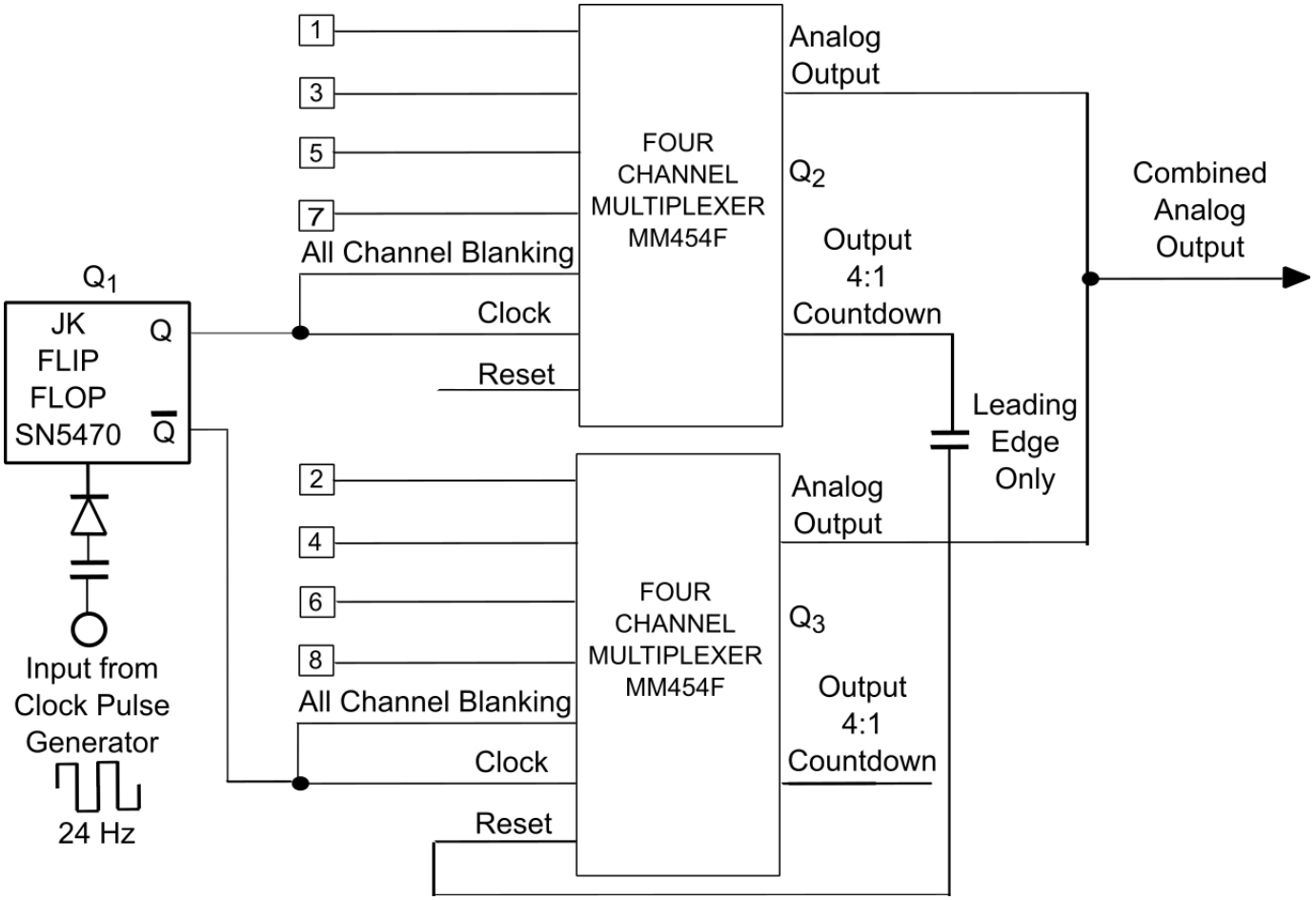


Figure 17: Multiplexer

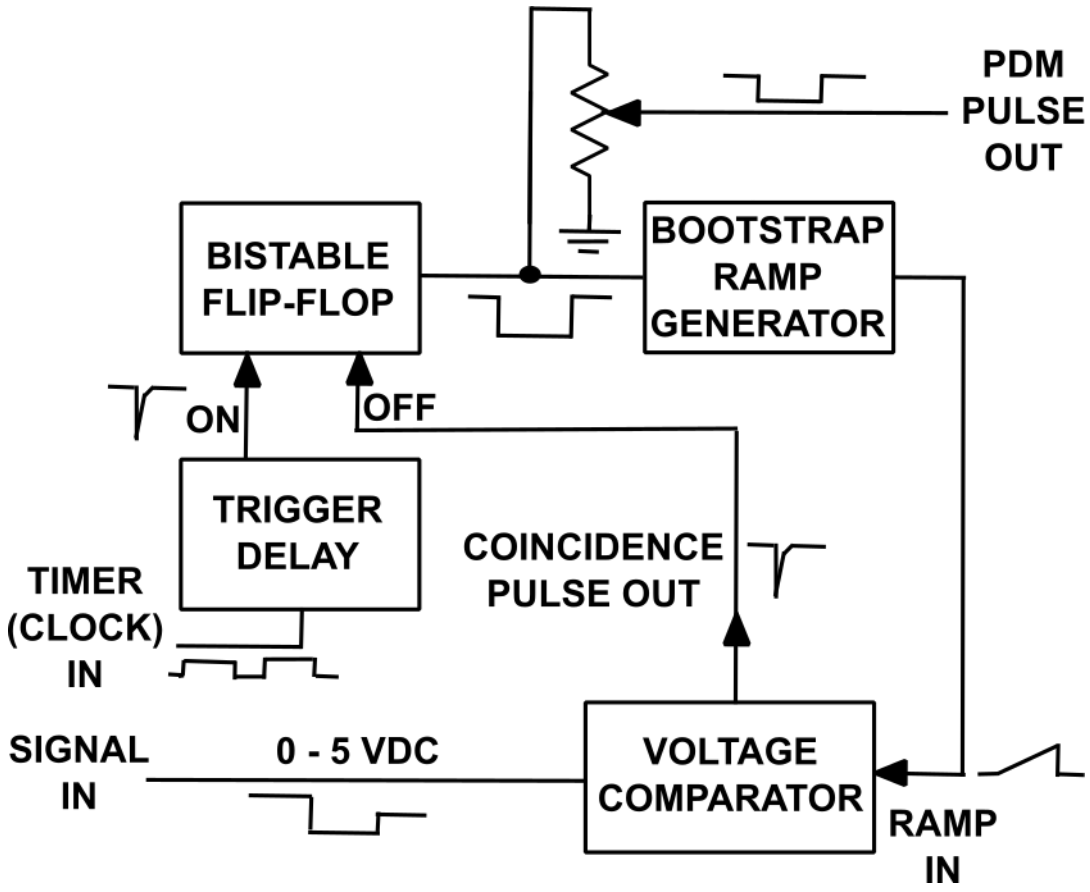


Figure 18: Pulse Duration Modulator Block Schema

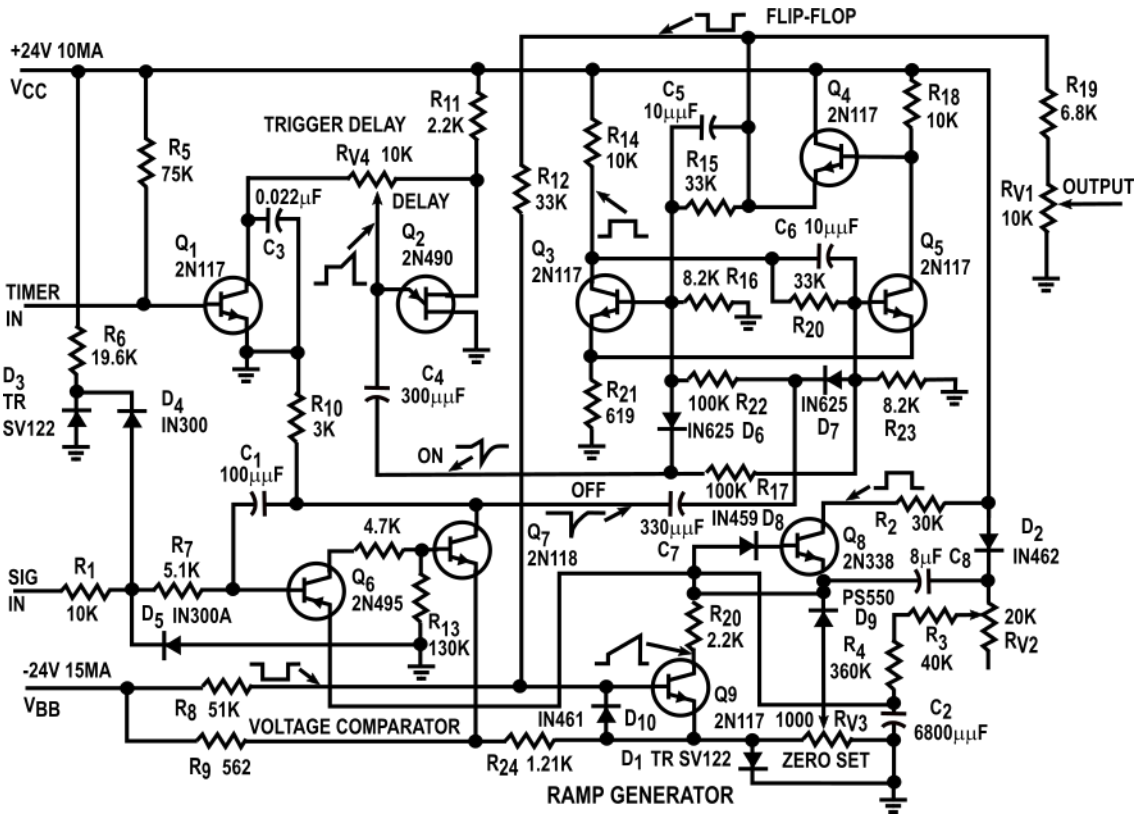


Figure 19: Pulse Duration Modulator 900 Hz

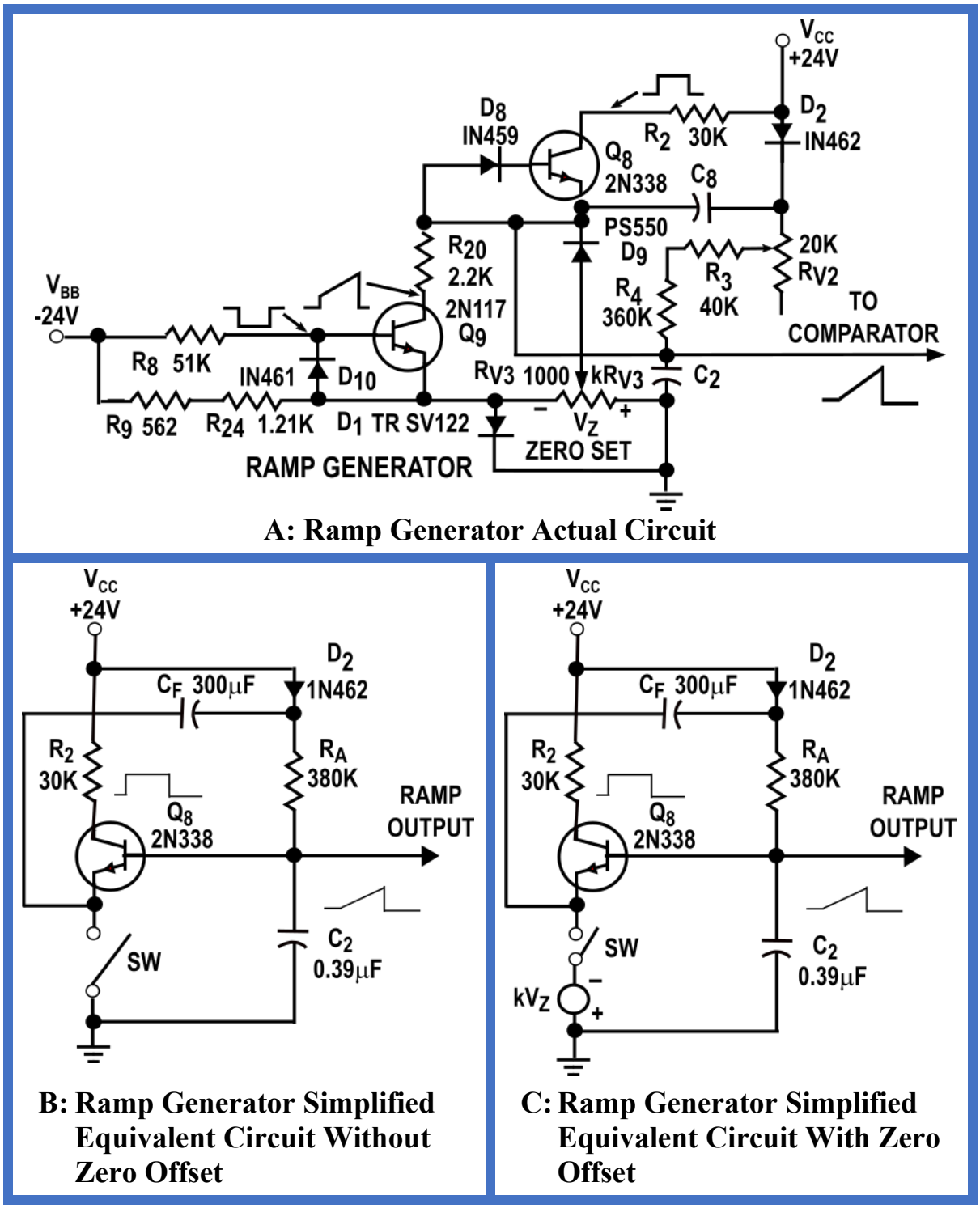
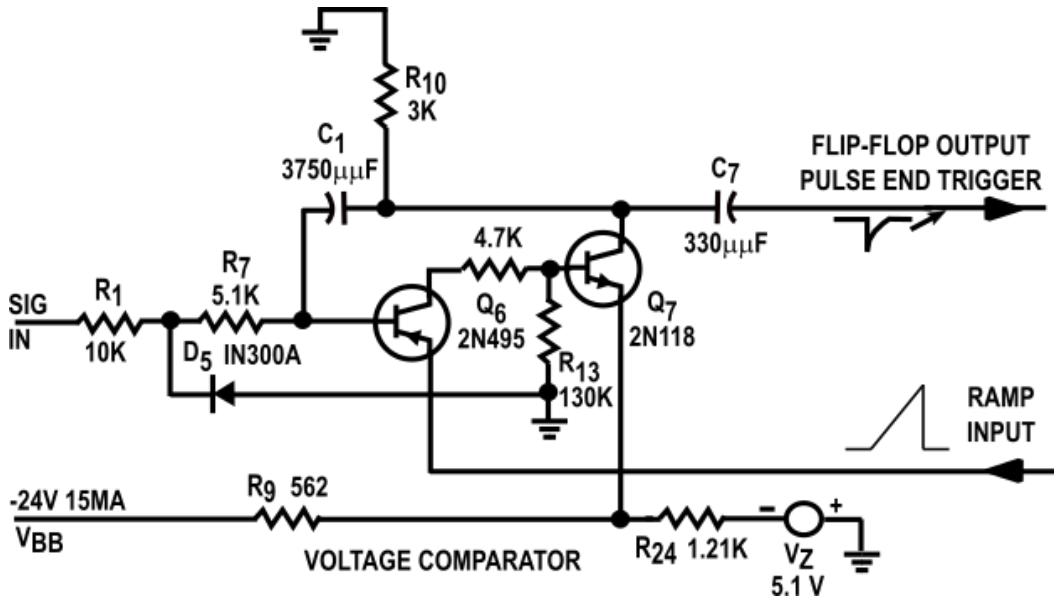
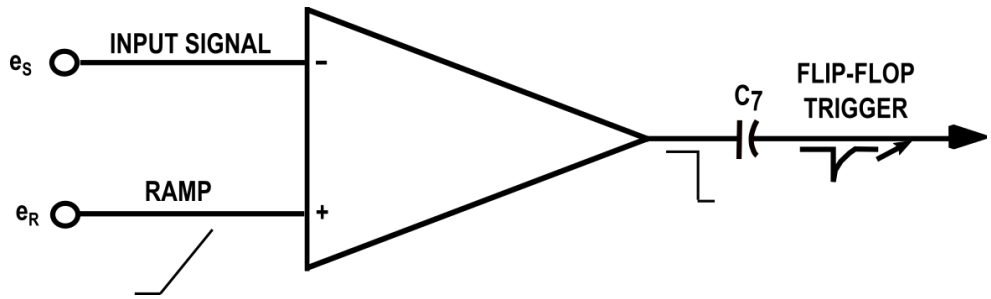


Figure 20: Pulse Duration Modulator Ramp Generator



A: Voltage Comparator Circuit



B: Voltage Comparator Simplified Equivalent Circuit

Zero Offset (Int/Ext)	Ext Offset Range	Input Signal Range	Int Offset Range	Ramp Signal Range
Int	0	0 to 5.0 V	--0.455 to 0.0 V	--0.455 to 5.0 V
Ext	0.0 to 0.417 V	0.417 to 5.0 V	0	0 to 5.0 V

C: Voltage Comparator Input and Ramp Signal Ranges

Figure 21: Pulse Duration Modulator Voltage Comparator

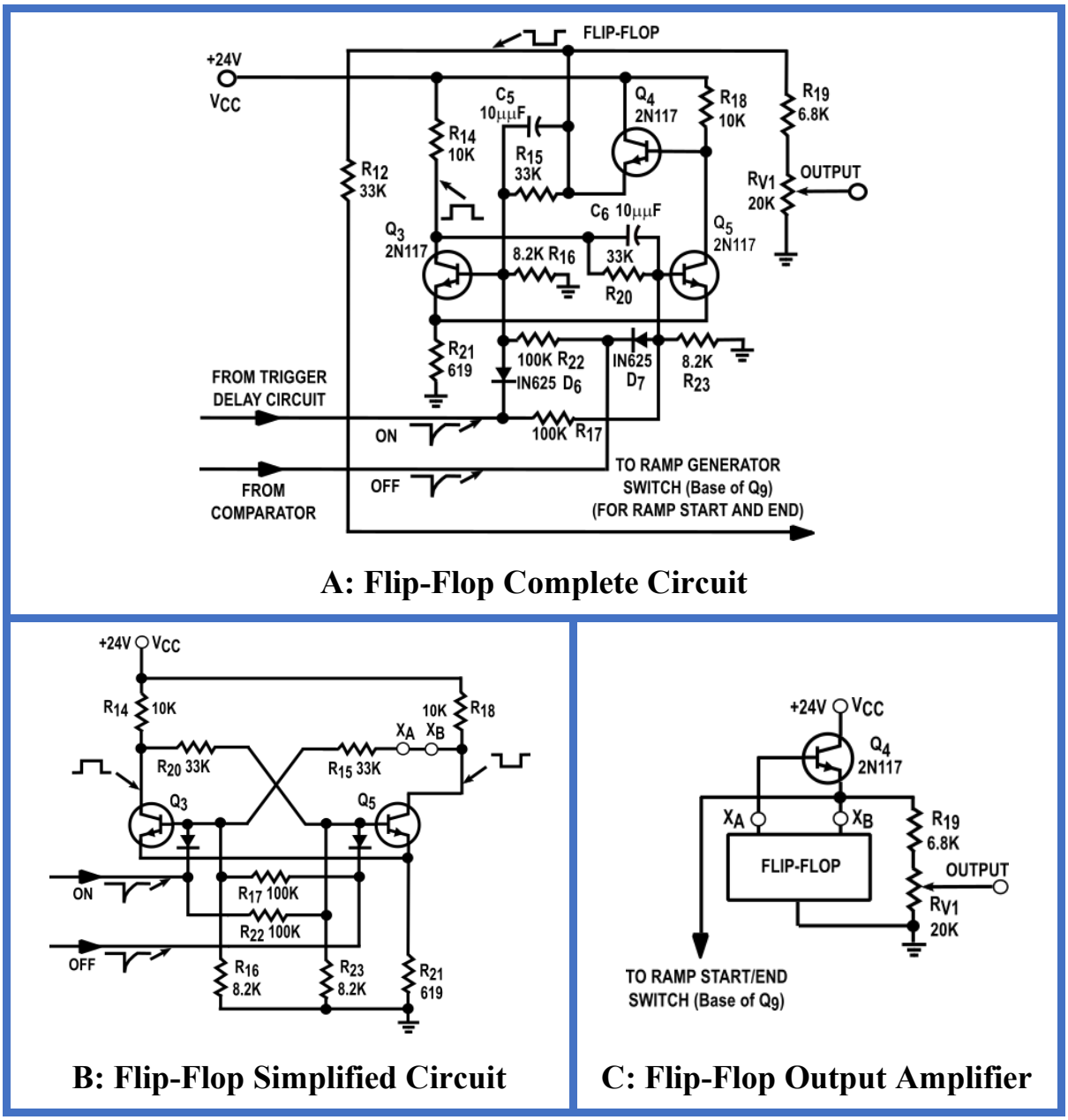


Figure 22: Pulse Duration Modulator Flip-Flop

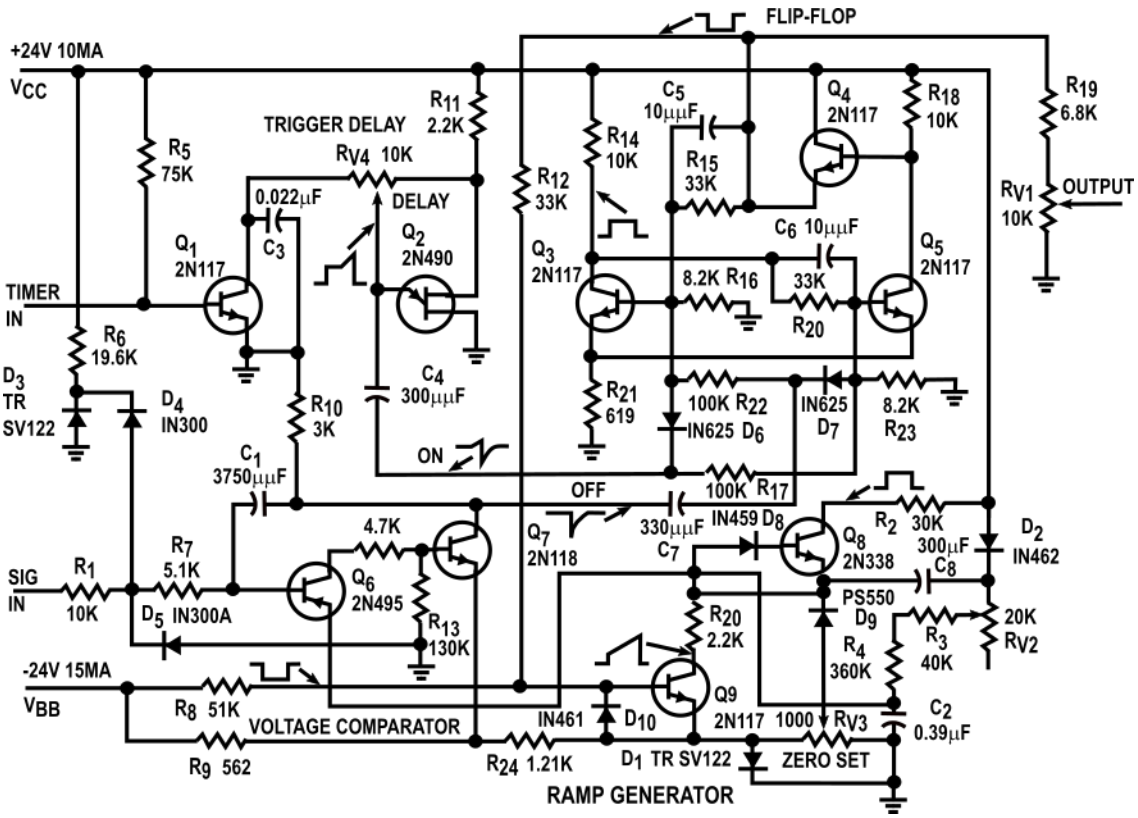


Figure 23: Flight Memory Pulse Duration Modulator 24 Hz

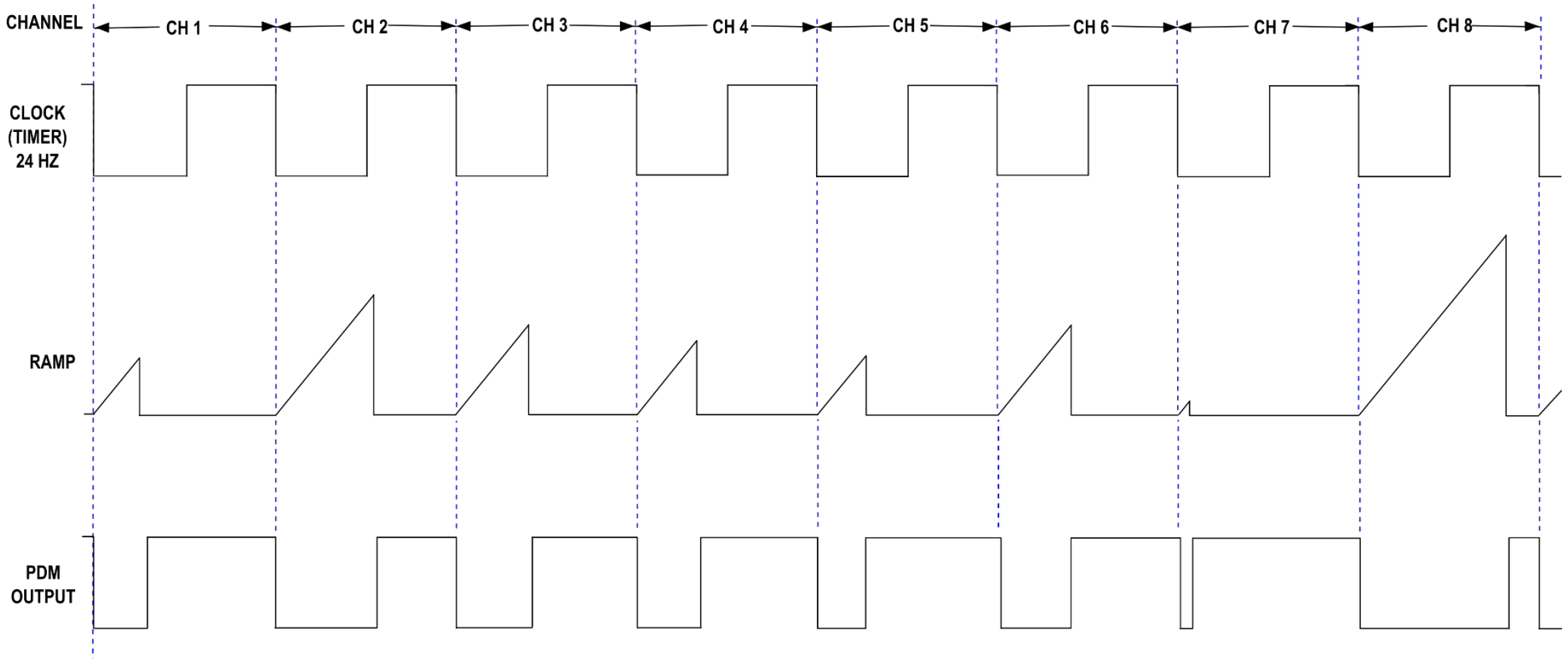
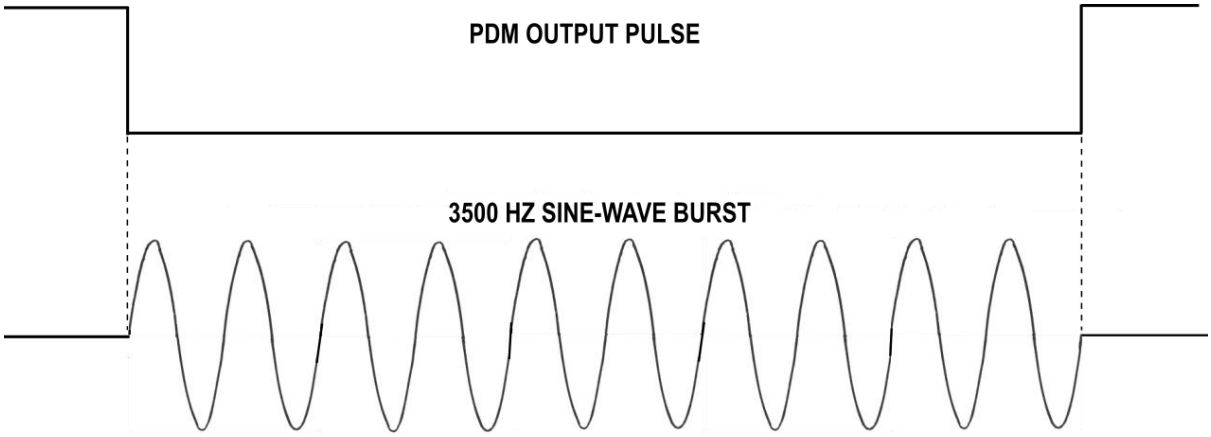


Figure 24: Pulse Duration Modulator Graphs

A: Pulse and 10-Cycle Sine Detailed Graph



B. Gated 3500 Hz Sine-Wave Equivalent Circuit

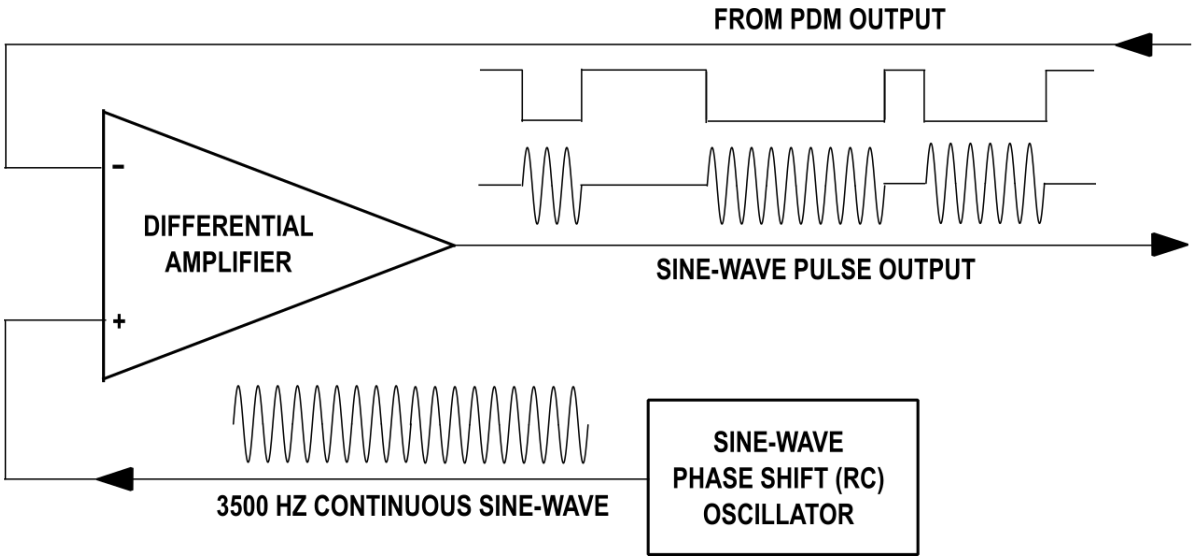
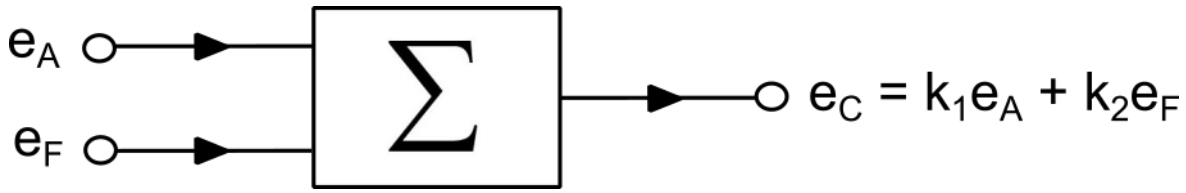
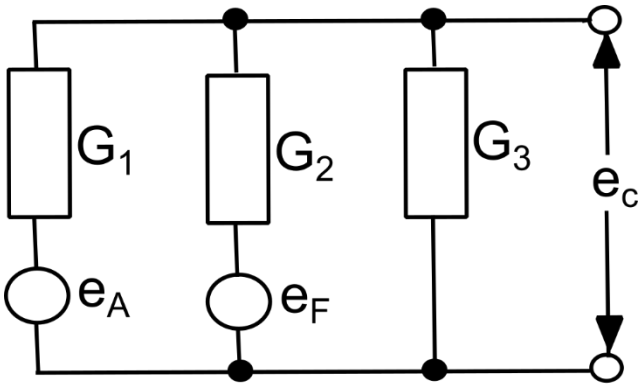


Figure 25: Sine-Wave Amplitude Modulator



A: Combiner Simplified Block Schema



$$e_c = \frac{e_A G_1 + e_F G_2}{G_1 + G_2 + G_3}$$

$$k_1 = \frac{G_1}{G_1 + G_2 + G_3}$$

$$k_2 = \frac{G_2}{G_1 + G_2 + G_3}$$

B: Combiner Actual Circuit

Figure 26: Cockpit Voice and Flight Data Combiner

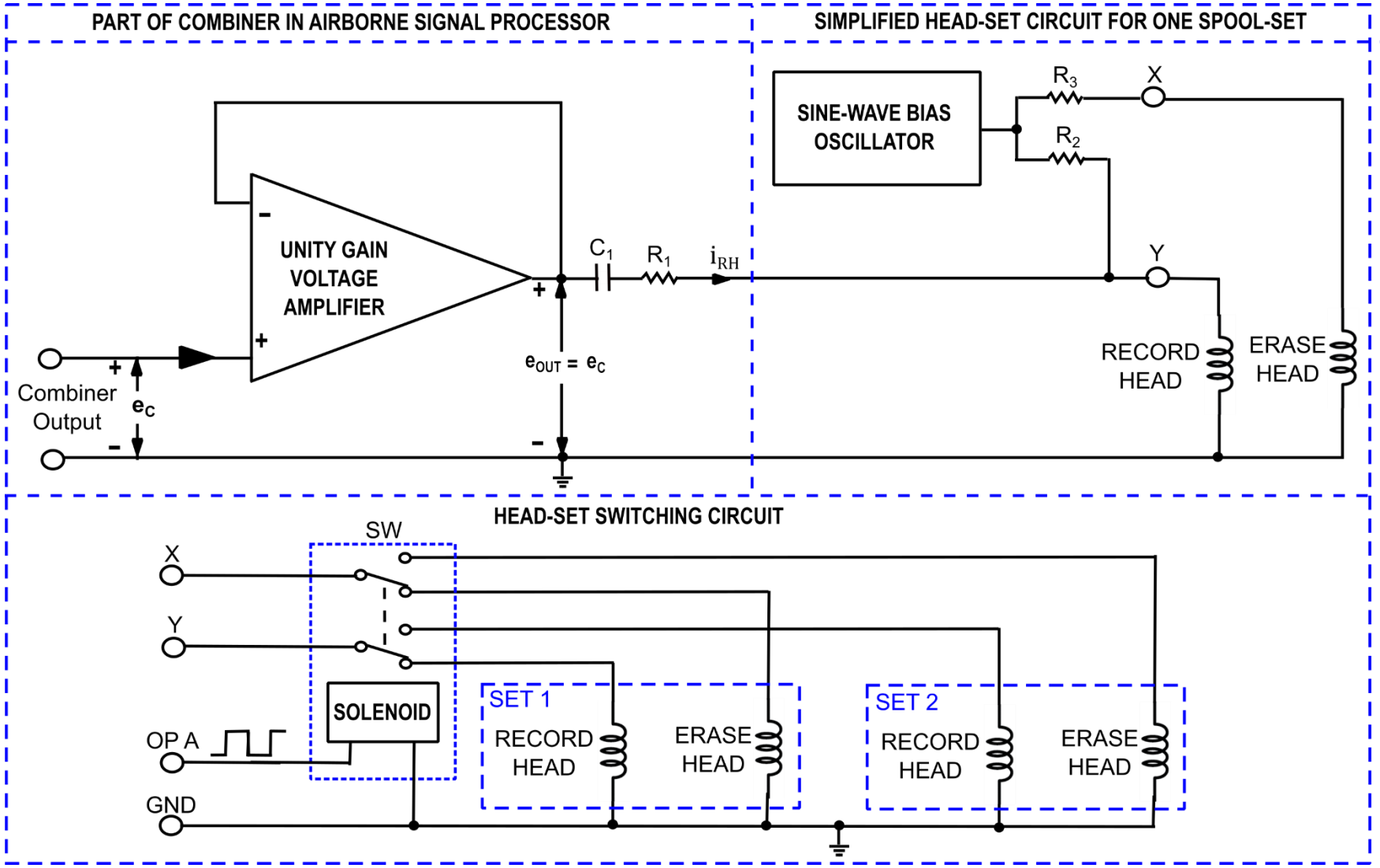


Figure 27: Simplified Airborne Recorder Input

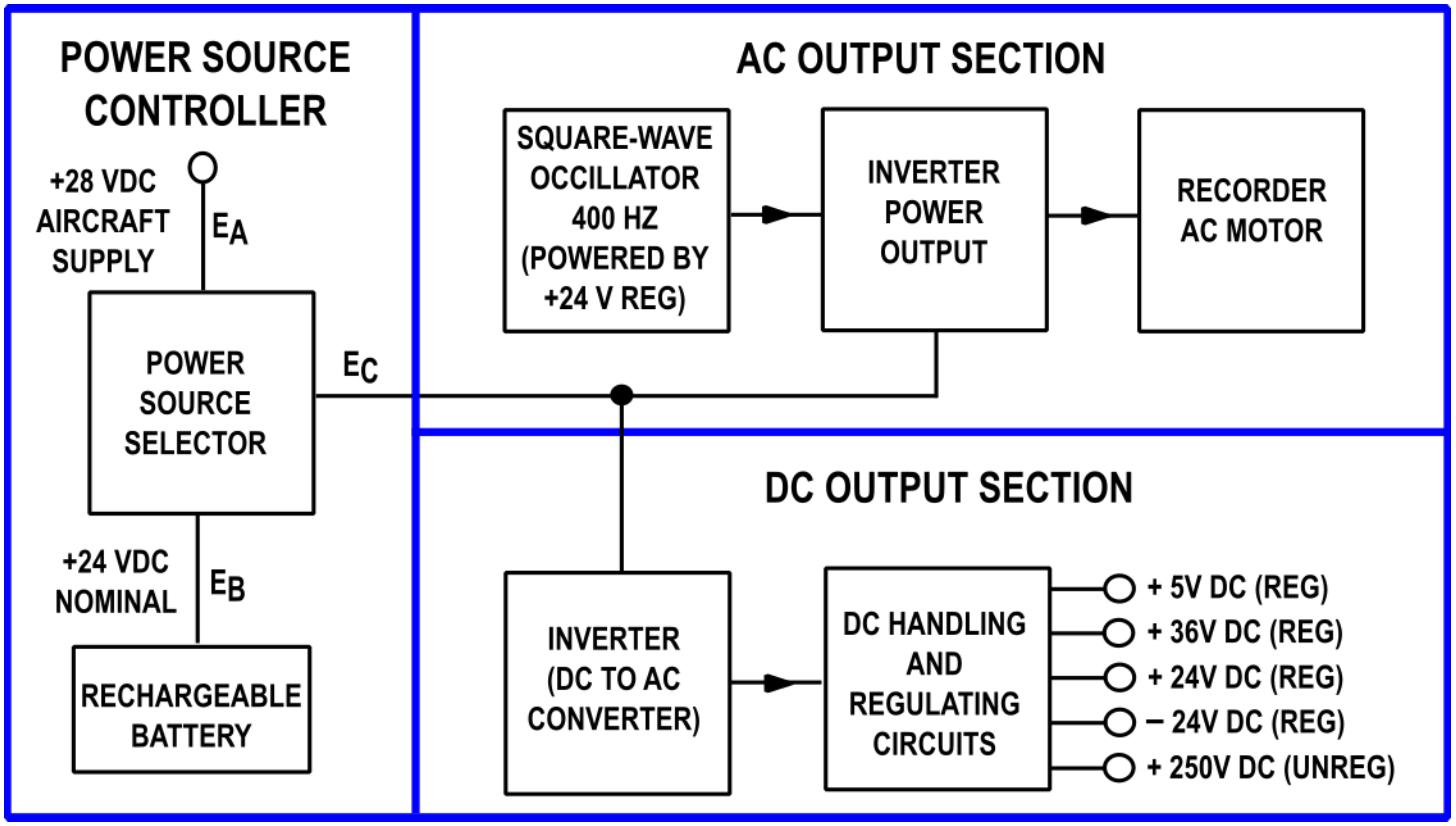


Figure 28: Airborne Power System Block Schema

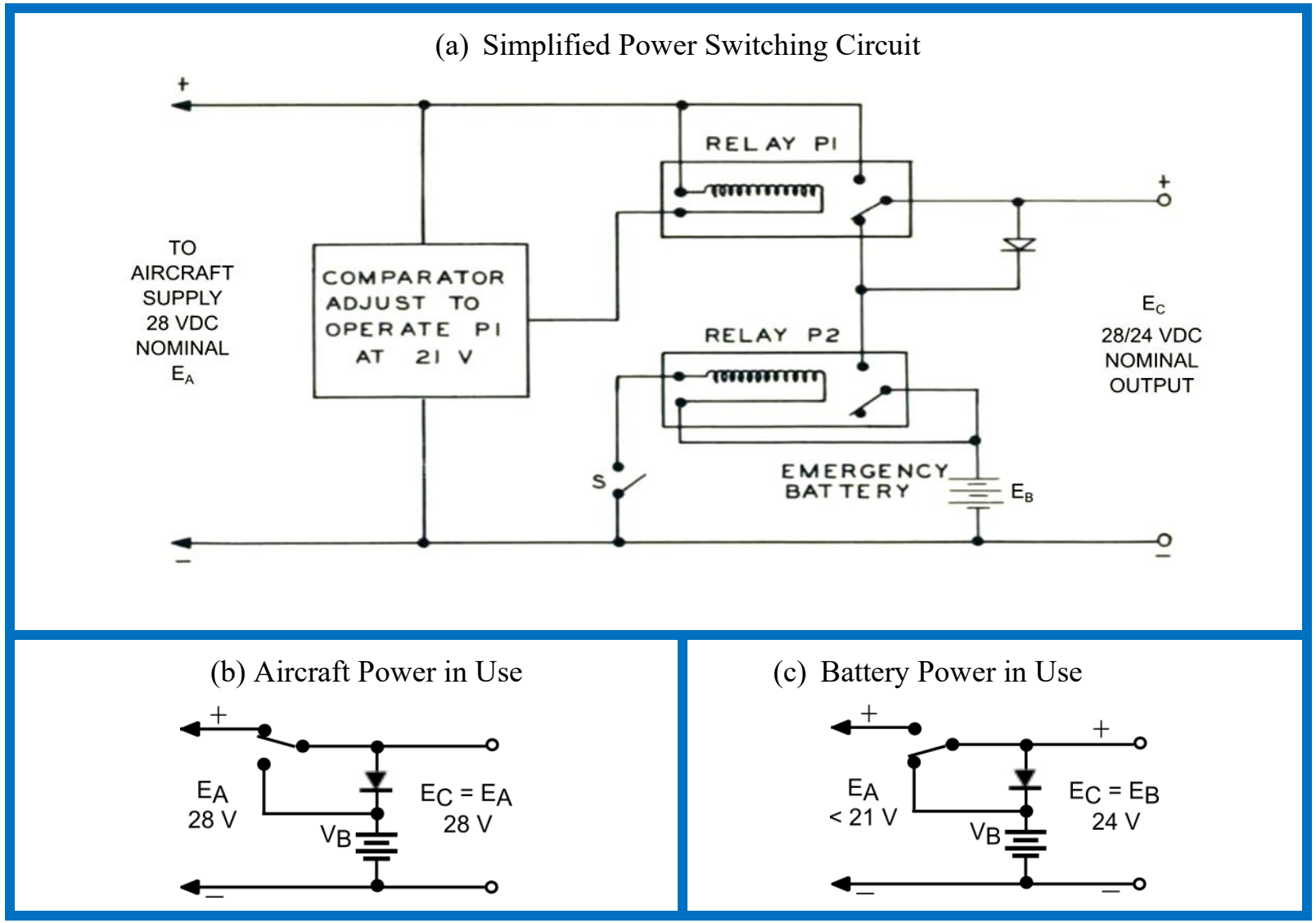


Figure 29: System of Switching from Aircraft to Emergency Supply

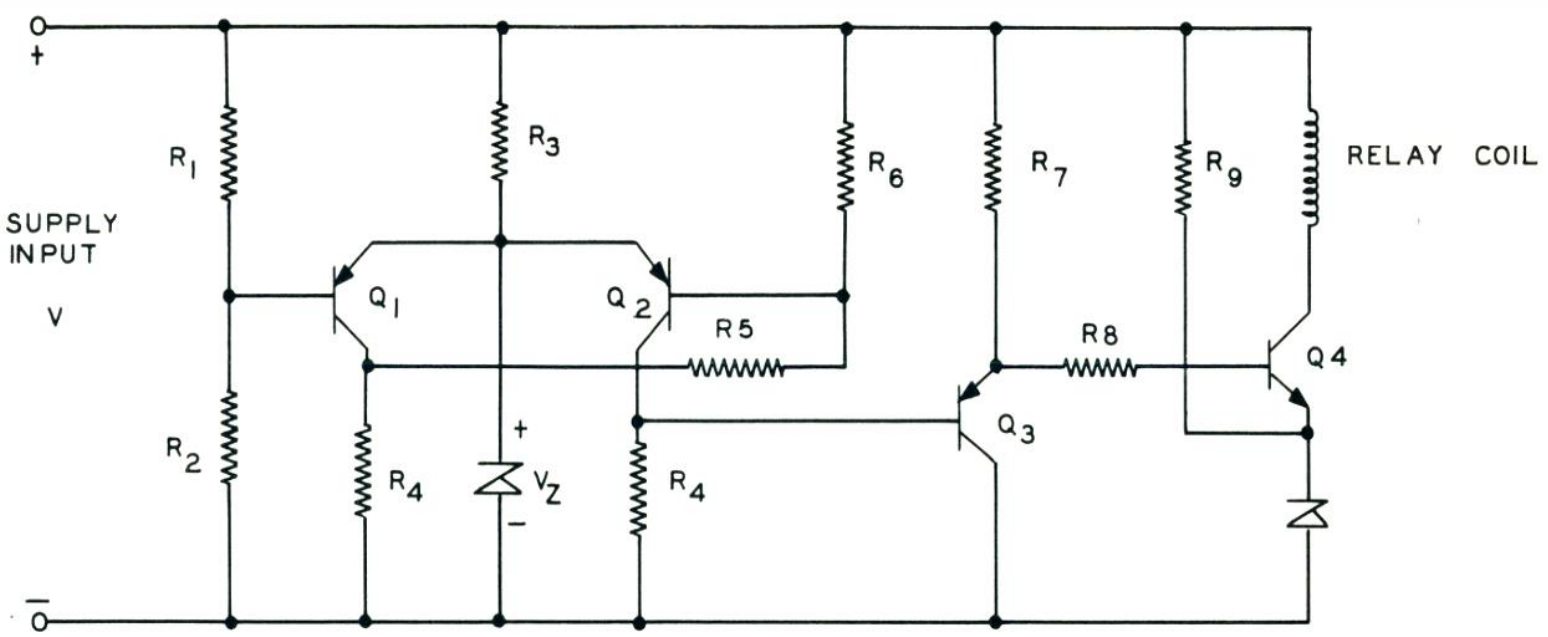


Figure 30: Basic Comparator Circuit

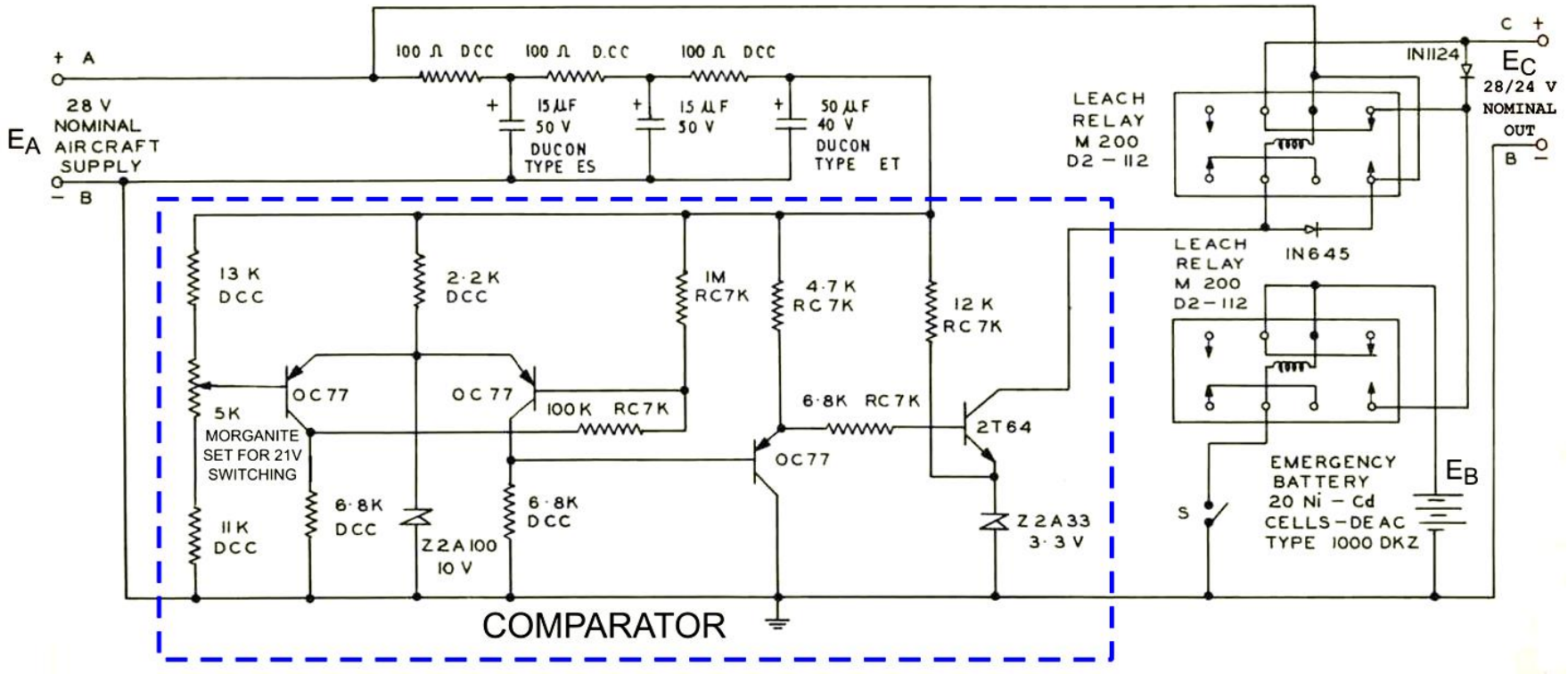


Figure 31: Complete Power System Switching Circuit

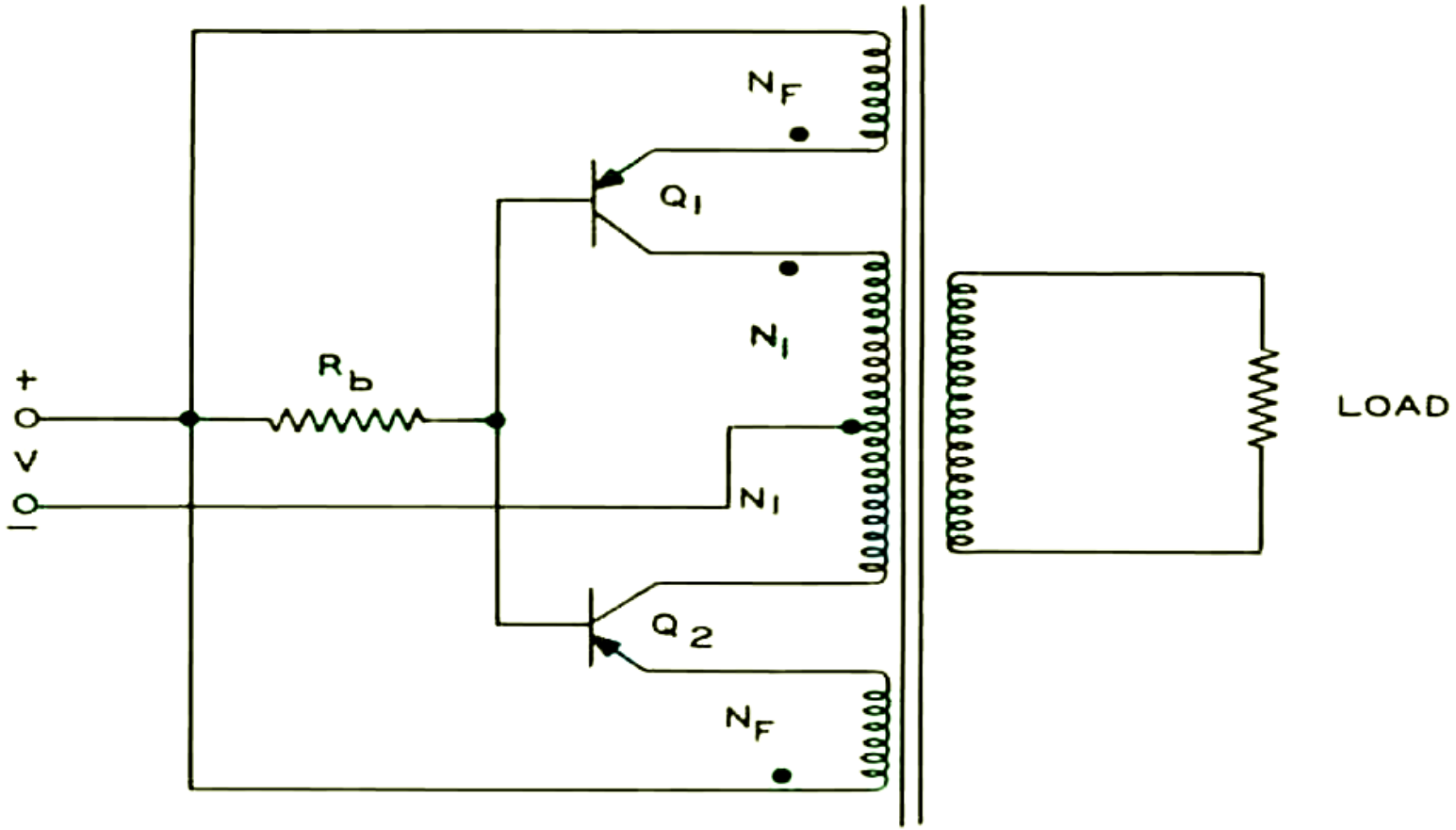


Figure 32: Common Base Inverter Circuit

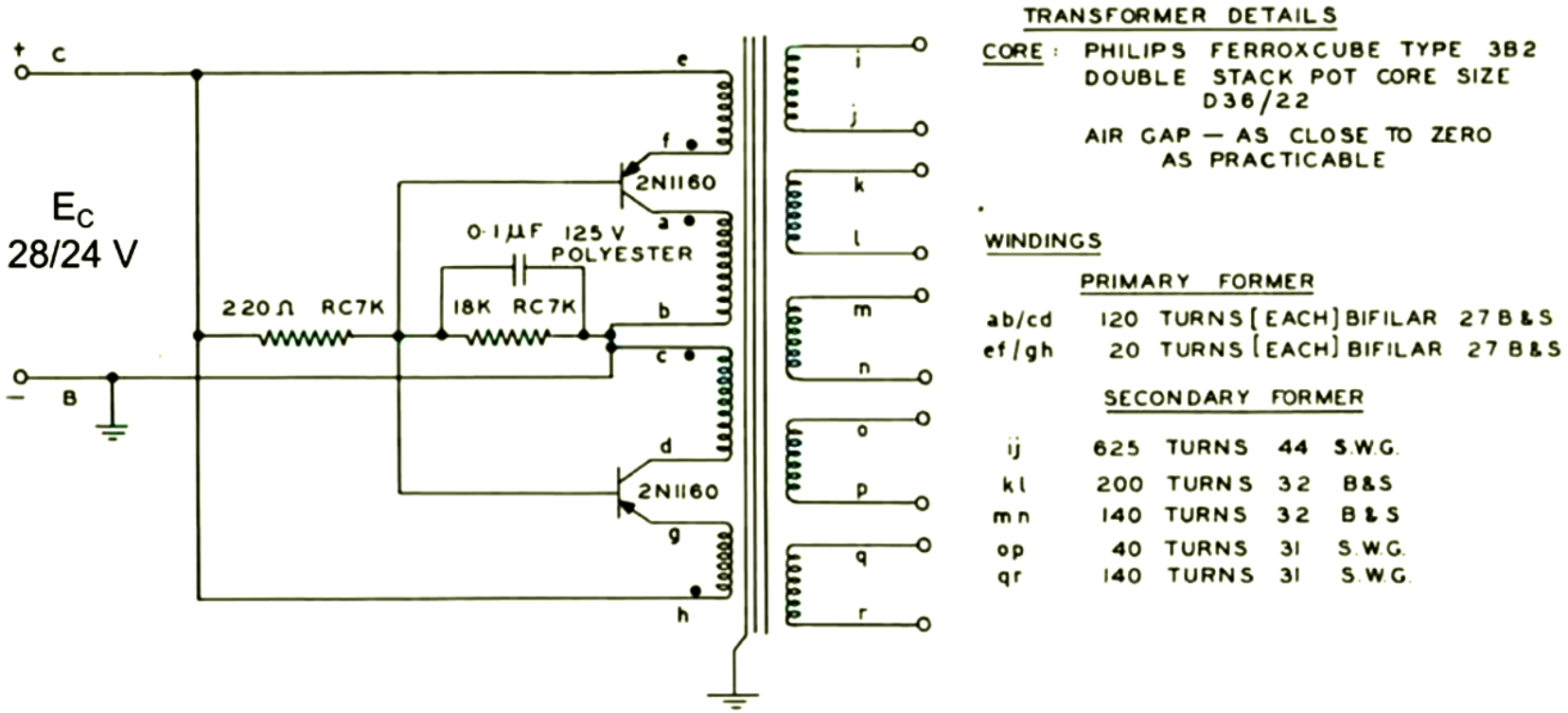


Figure 33: Inverter Circuit Details

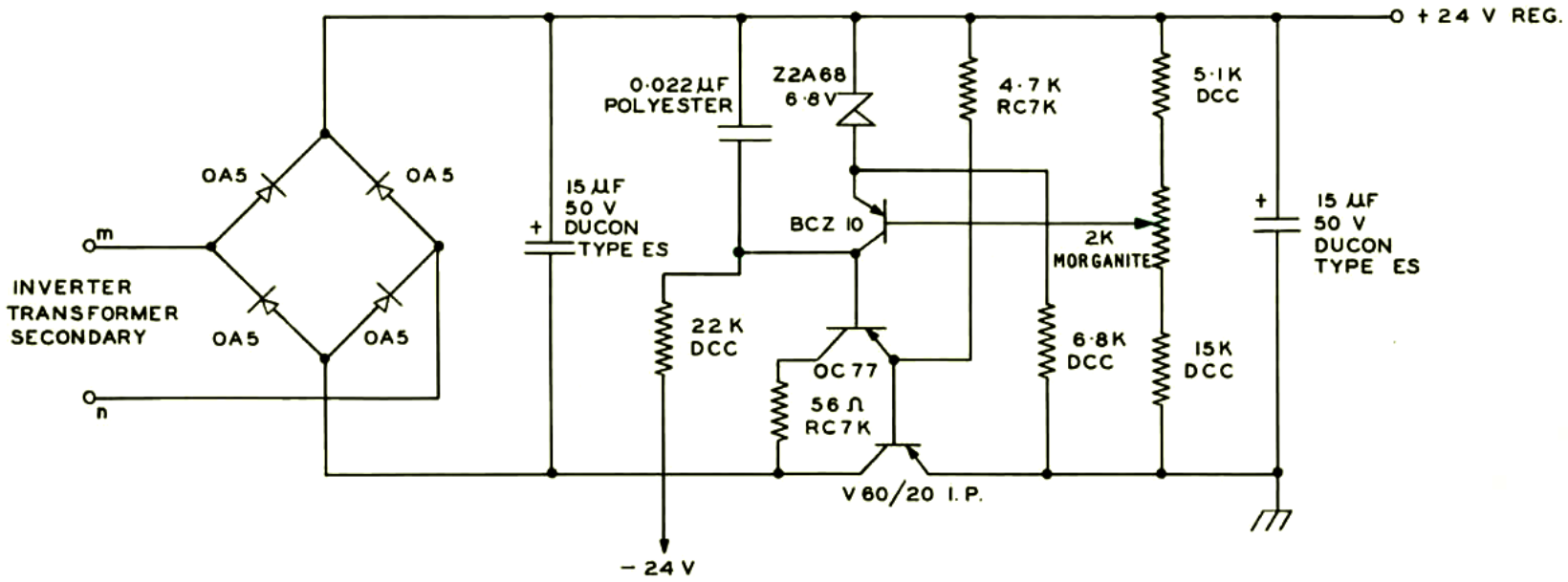


Figure 34: +24 V Regulator Complete Circuit

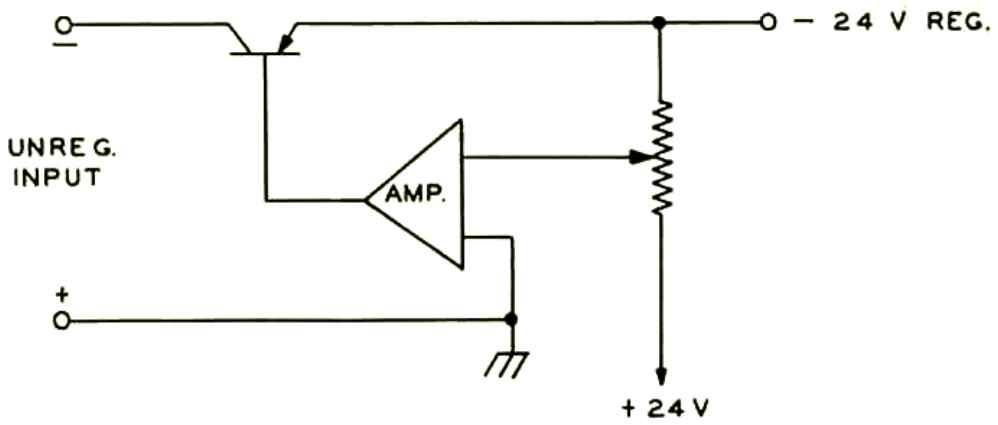


Figure 35a: Block Schema of –24 V Regulator

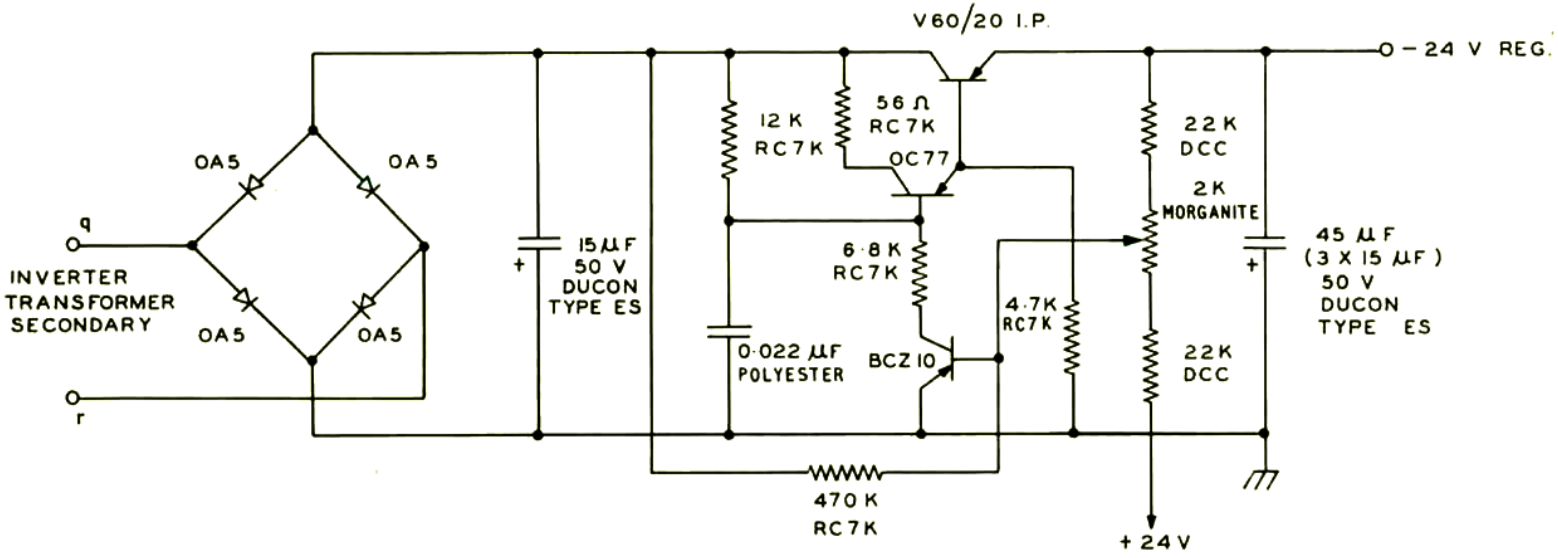


Figure 35b: –24 V Regulator Complete Circuit

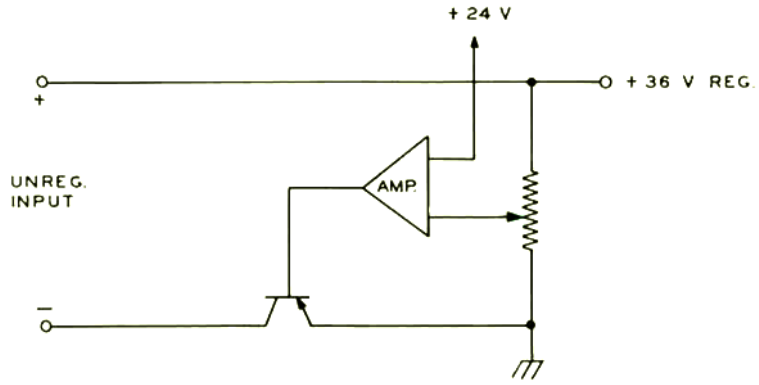


Figure 36a: Block Schema of +36 V Regulator

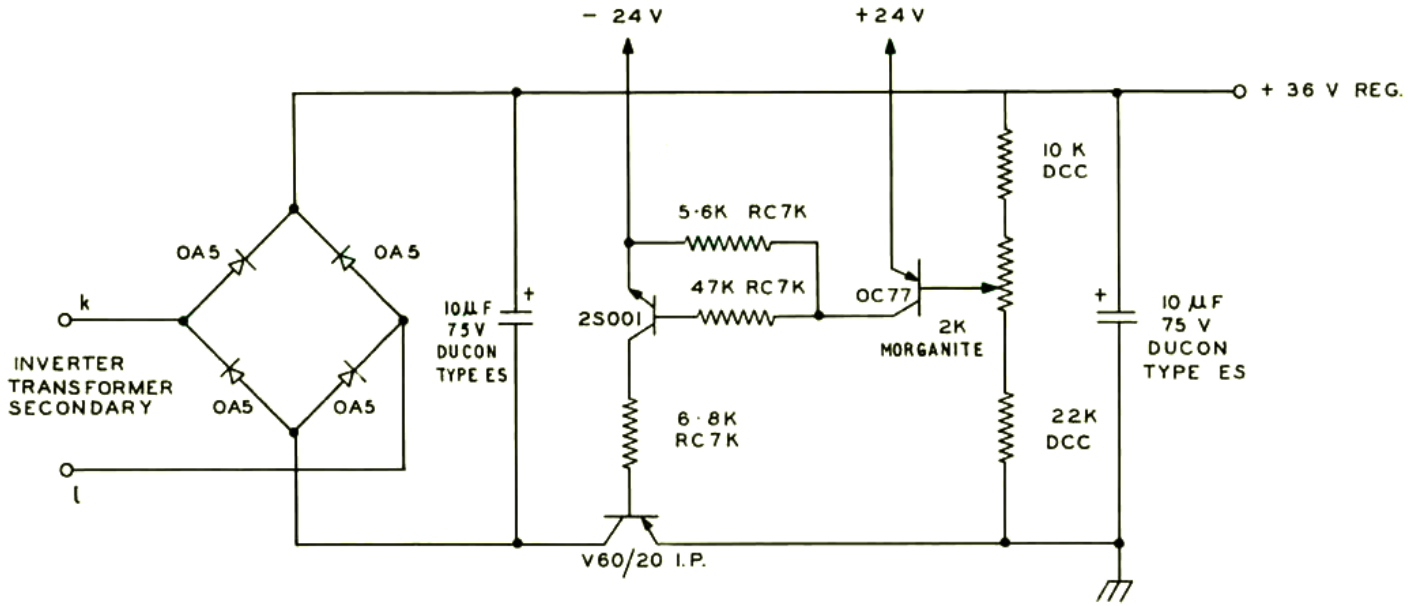


Figure 36b: +36 V Regulator Complete Circuit

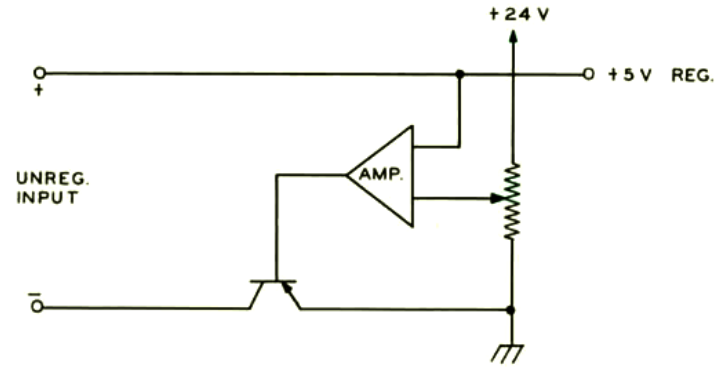


Figure 37a: Block Schema of +5 V Regulator

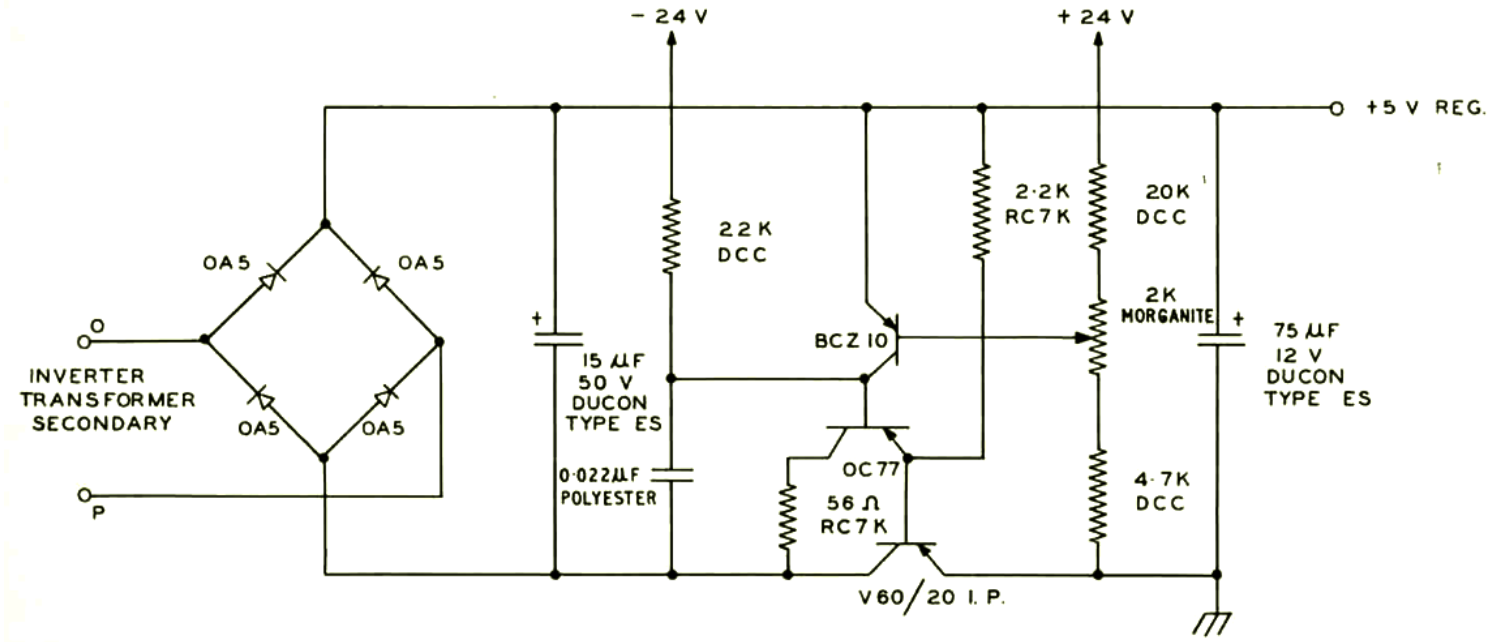


Figure 37b: +5 V Regulator Complete Circuit

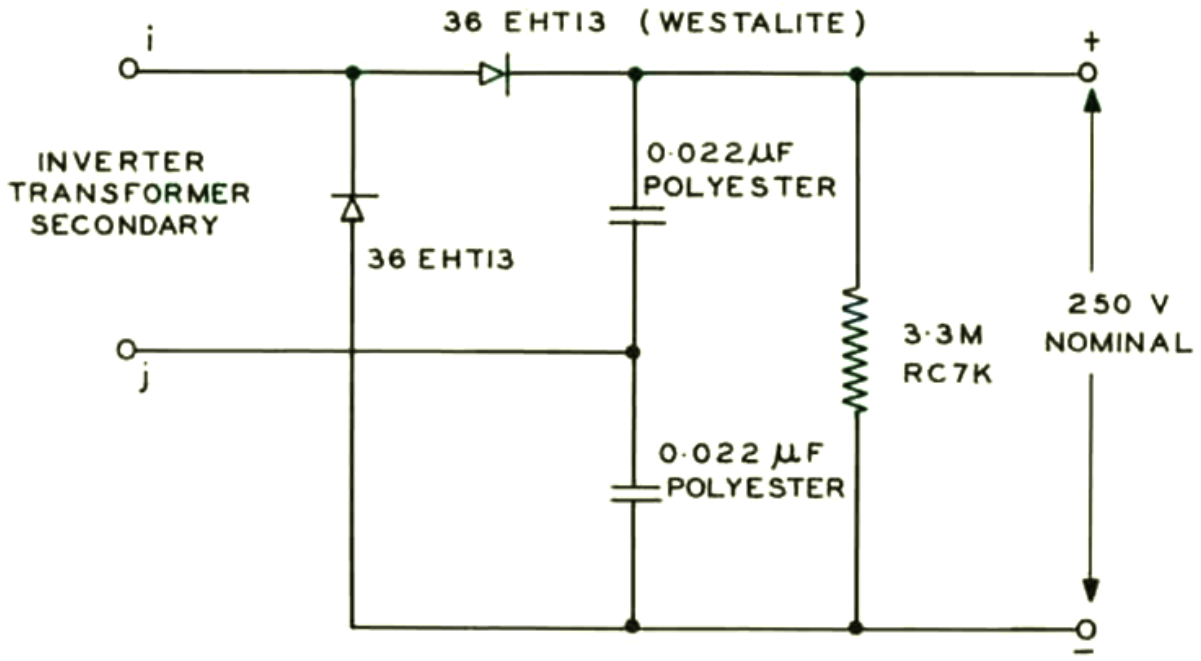


Figure 38: +250 V Unregulated Power Complete Circuit

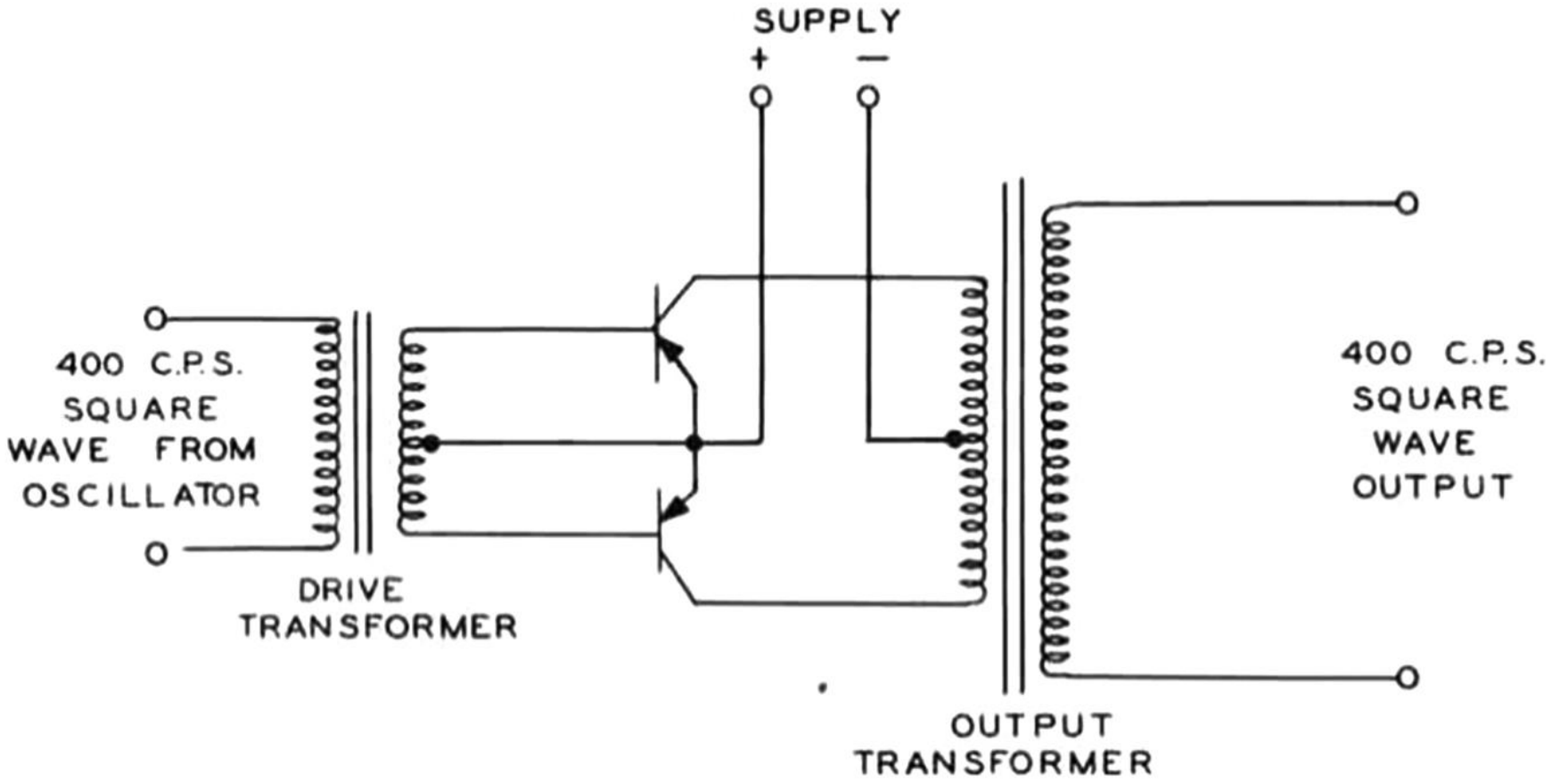


Figure 39: Typical Class B Output Stage

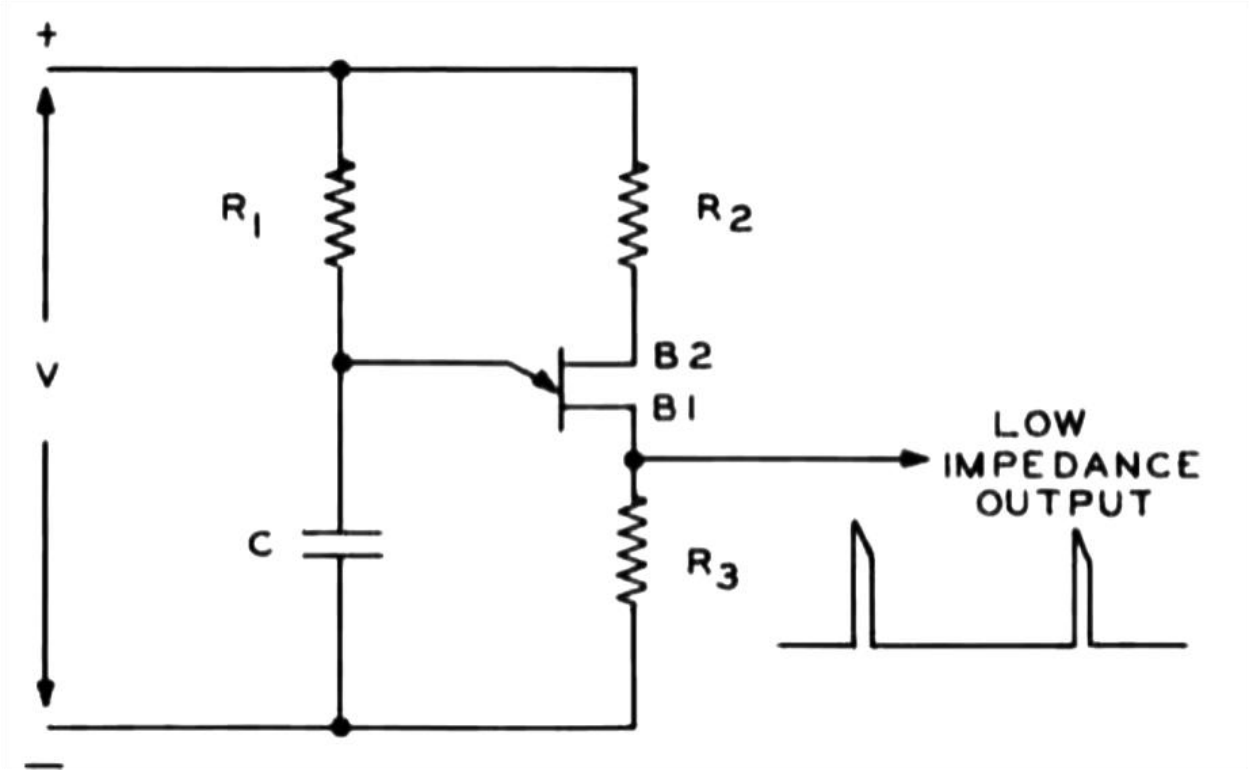


Figure 40: Basic Unijunction Transistor Relaxation Oscillator Circuit

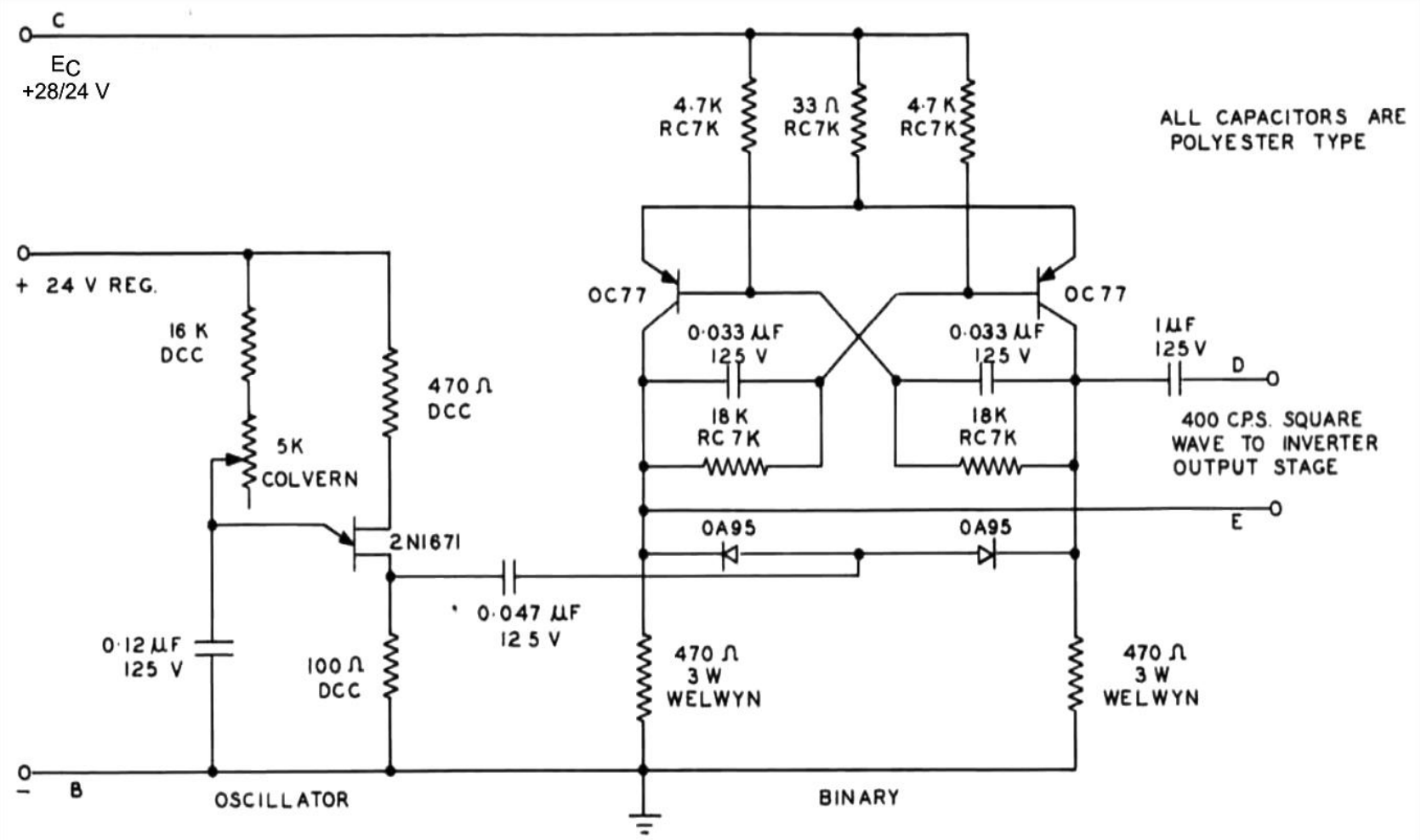


Figure 41: Circuit Details of Relaxation Oscillator with Square Wave Output

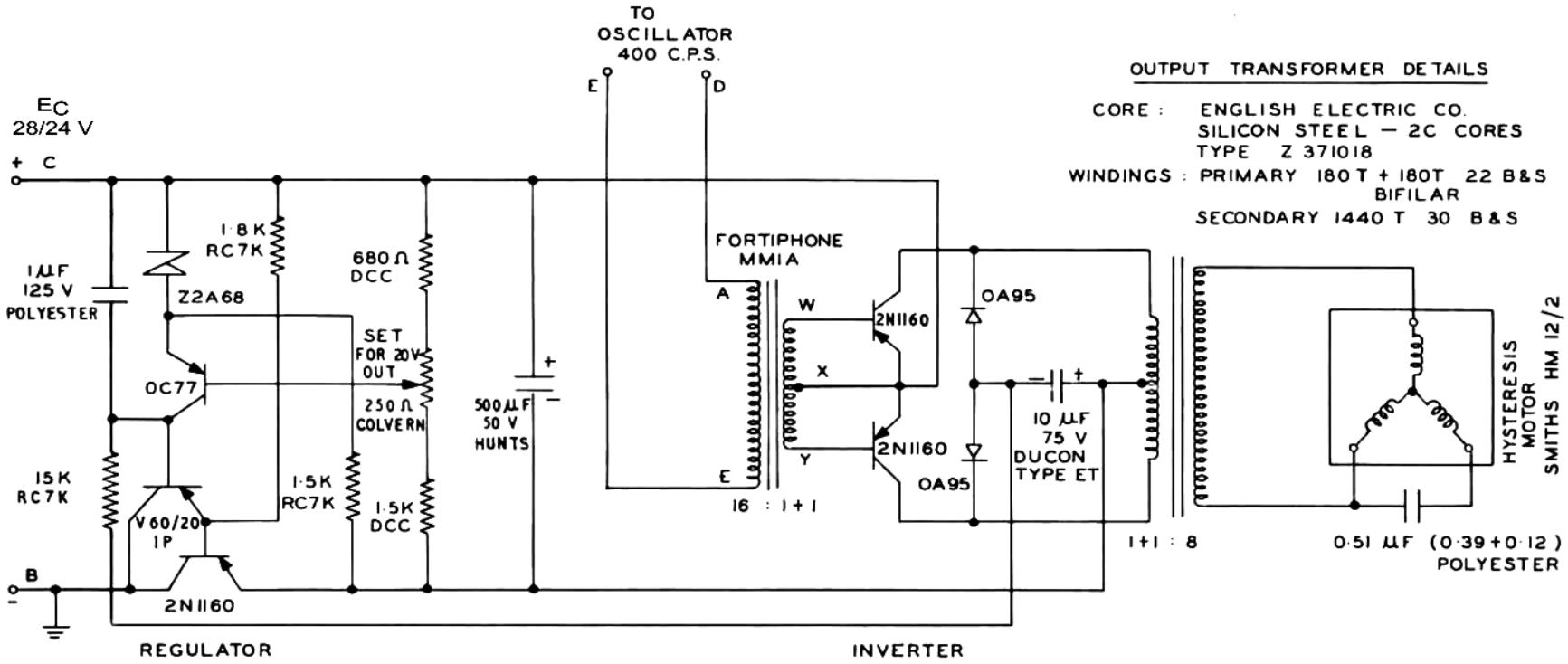


Figure 42: Circuit Details of Series Regulator and Inverter Output Stage

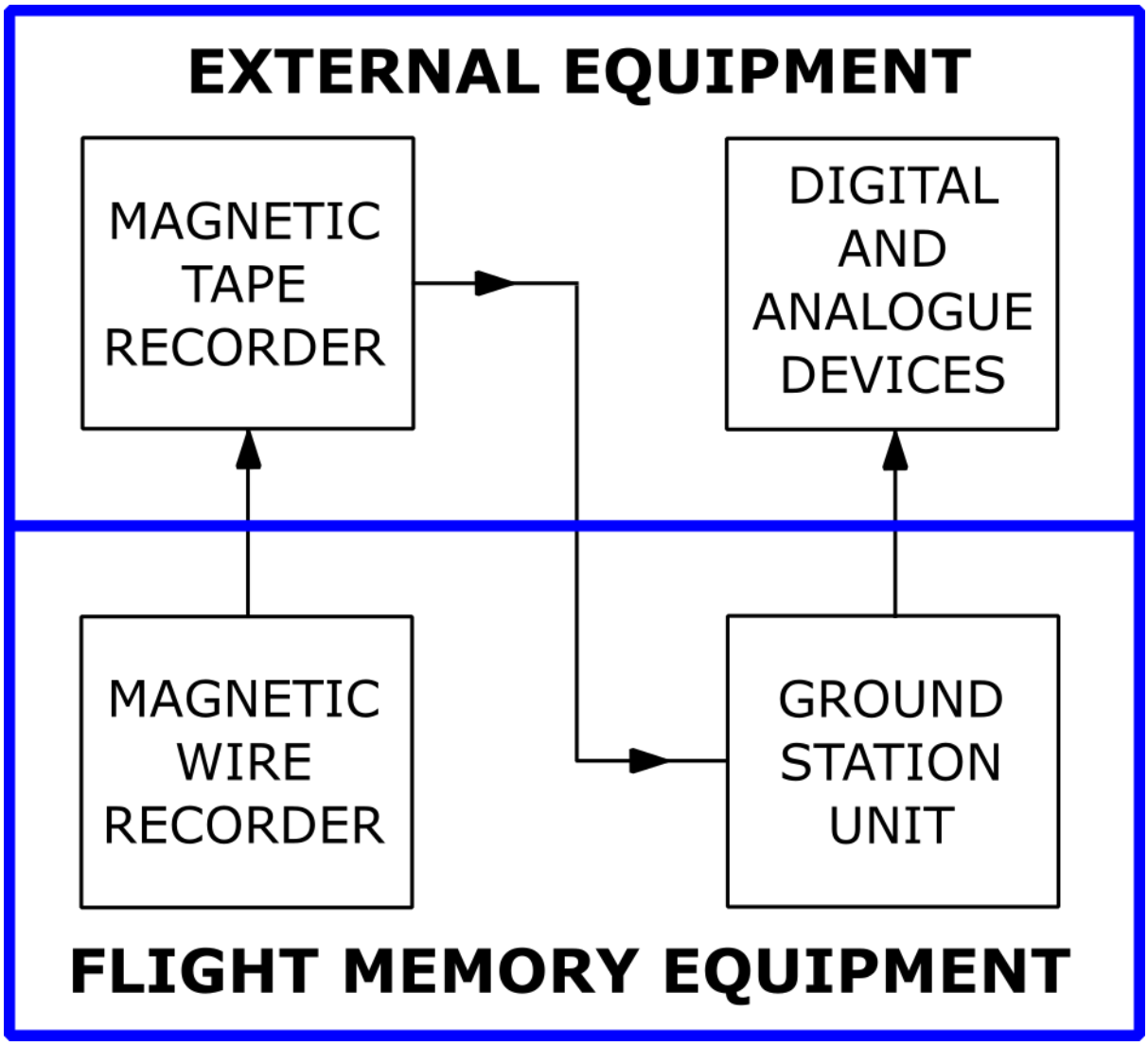


Figure 43: Simplified Ground System Block Schema

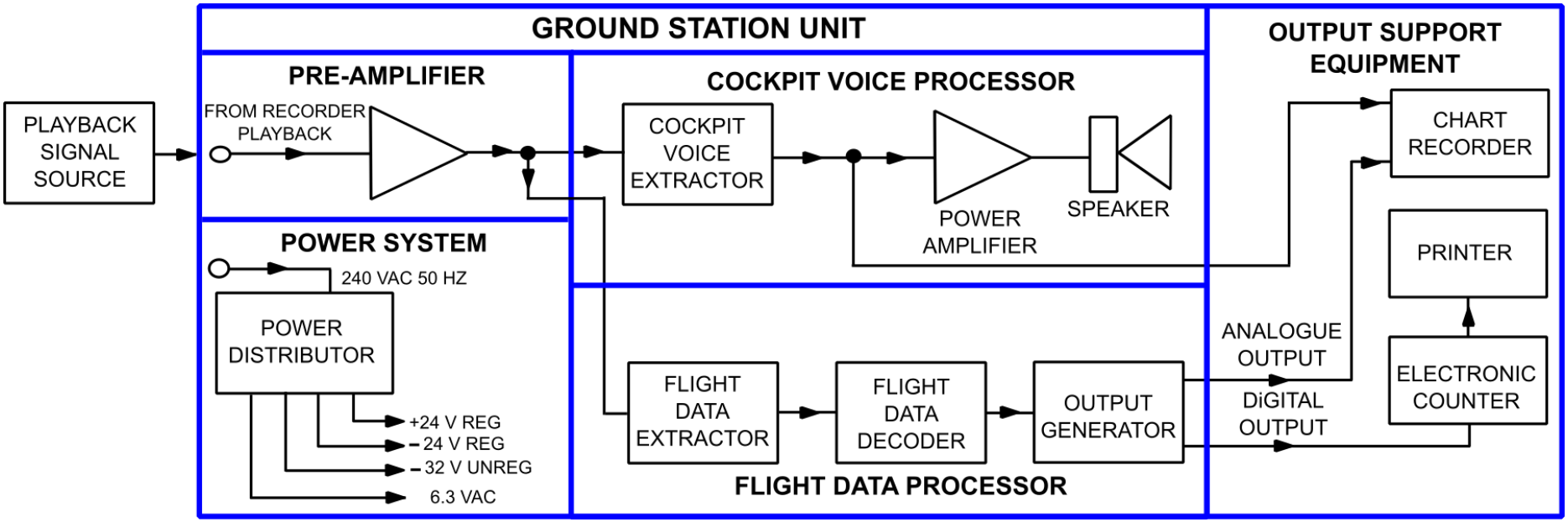


Figure 44: Ground Station Unit Block Schema Including External Output Devices

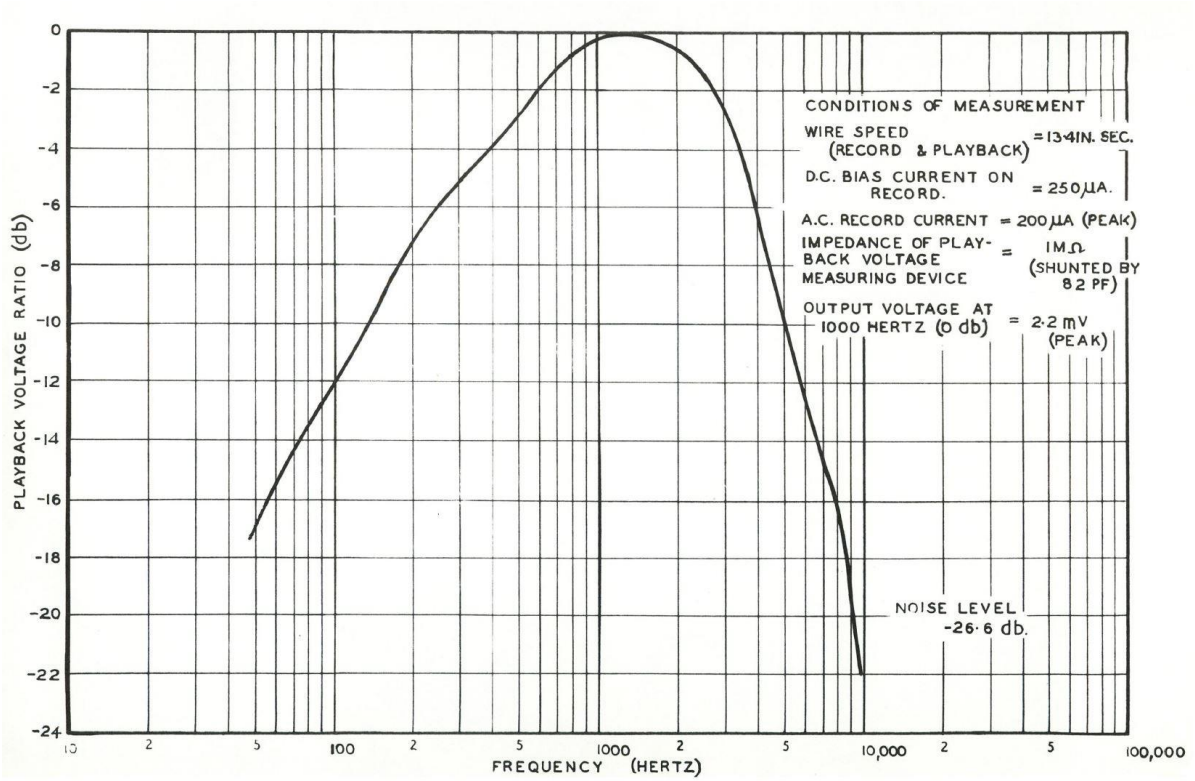


Figure 45: Frequency Response of Record/Playback Deck (Voltage on Playback for Constant Amplitude Record Current)

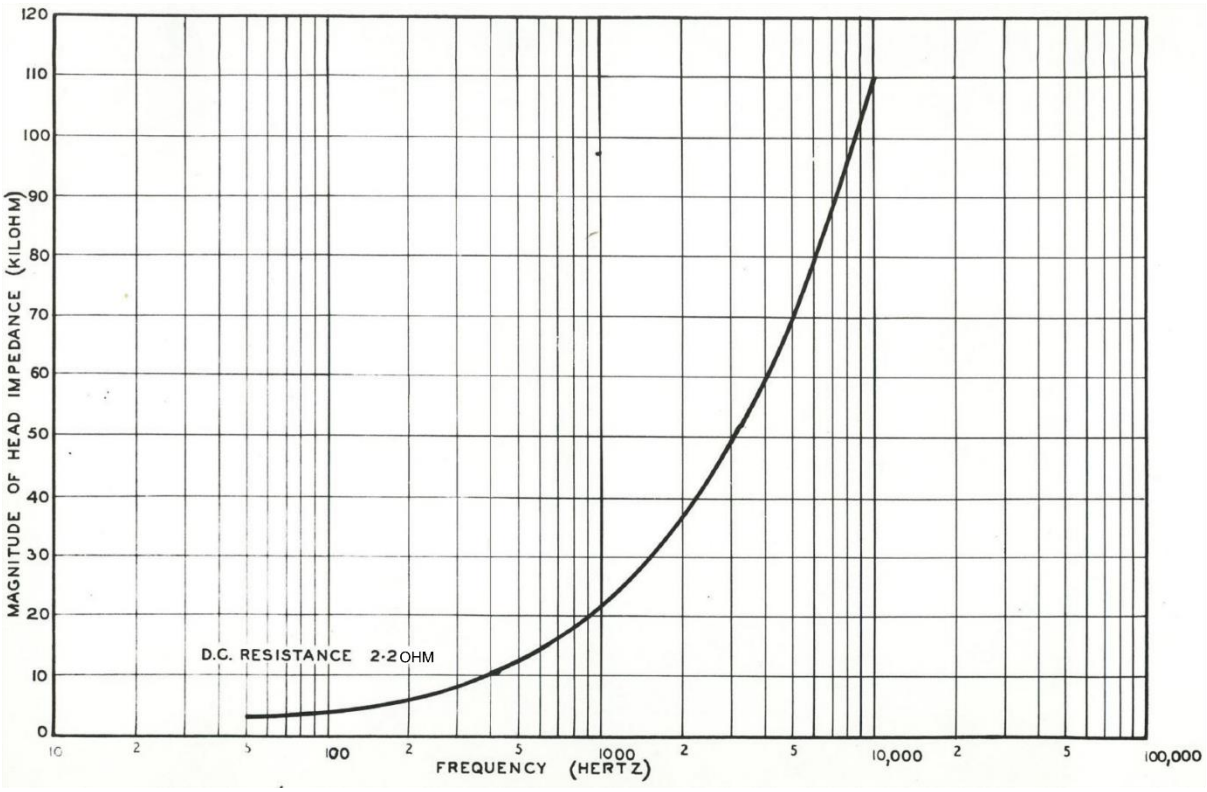


Figure 46: Record/Playback Head Impedance as a Function of Frequency

Figure 47: Front View of Ground Station Unit Within Box

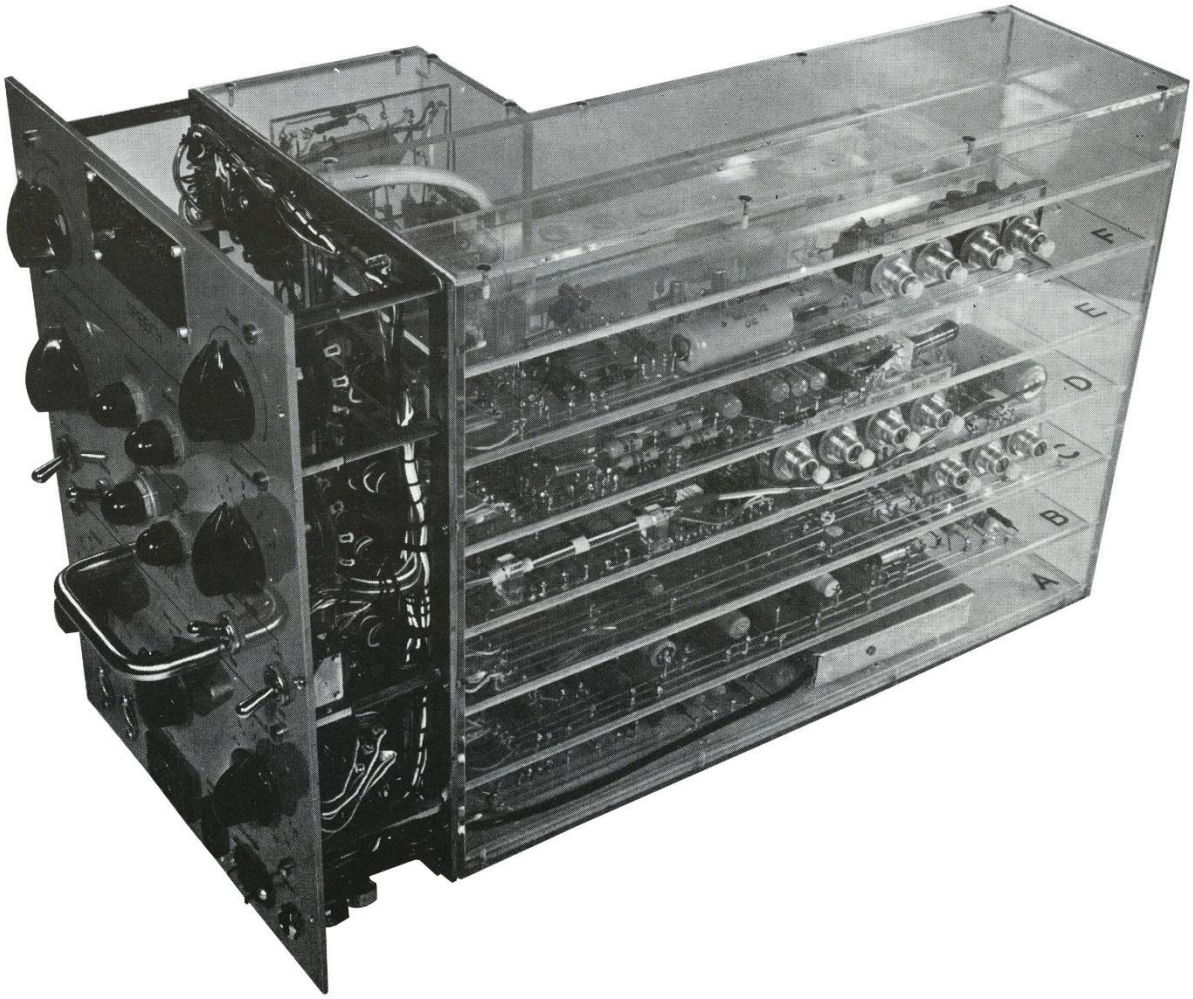


Figure 48: Right Hand Side View of Ground Station Unit

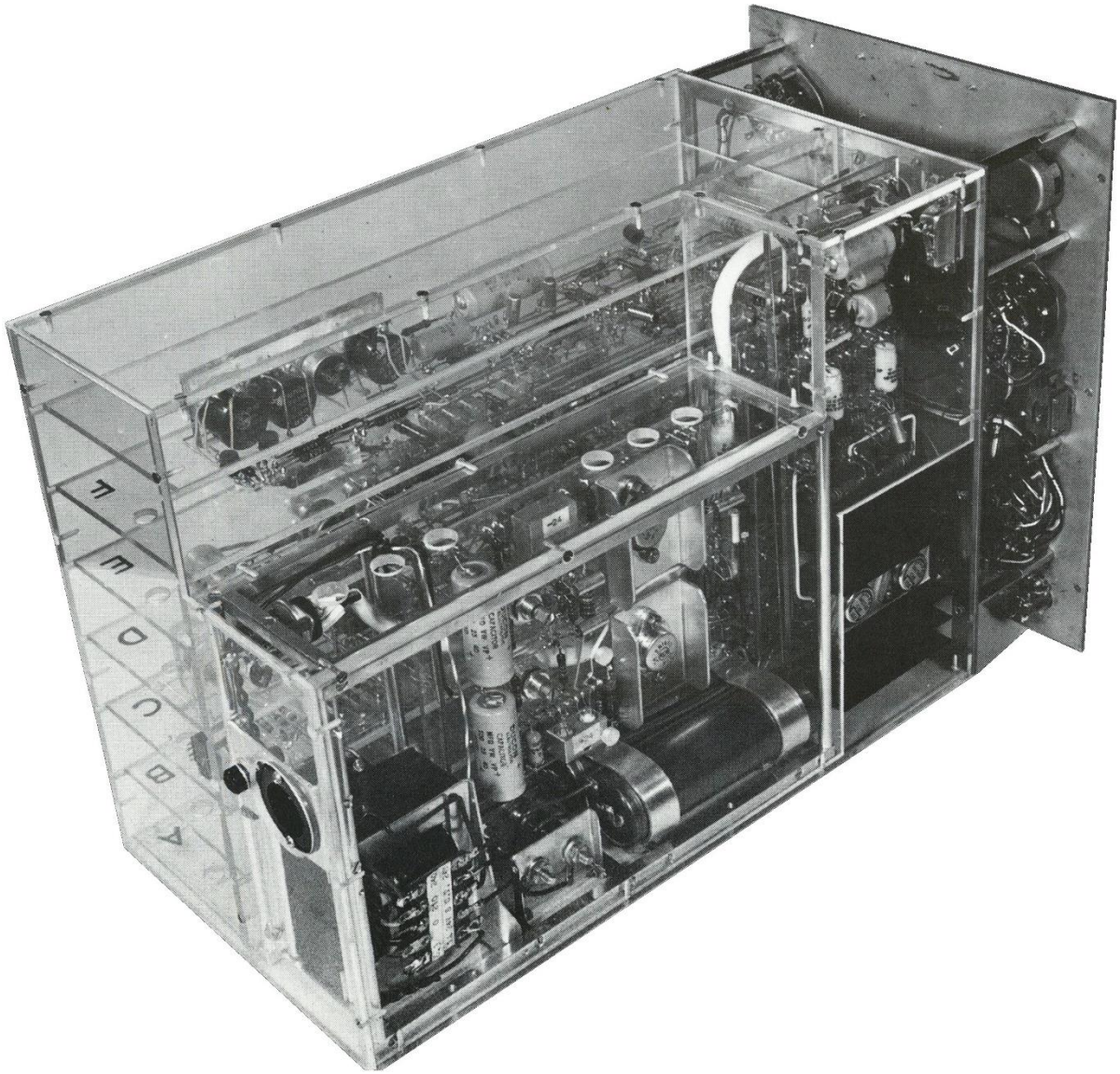


Figure 49: Left Hand Side View of Ground Station Unit

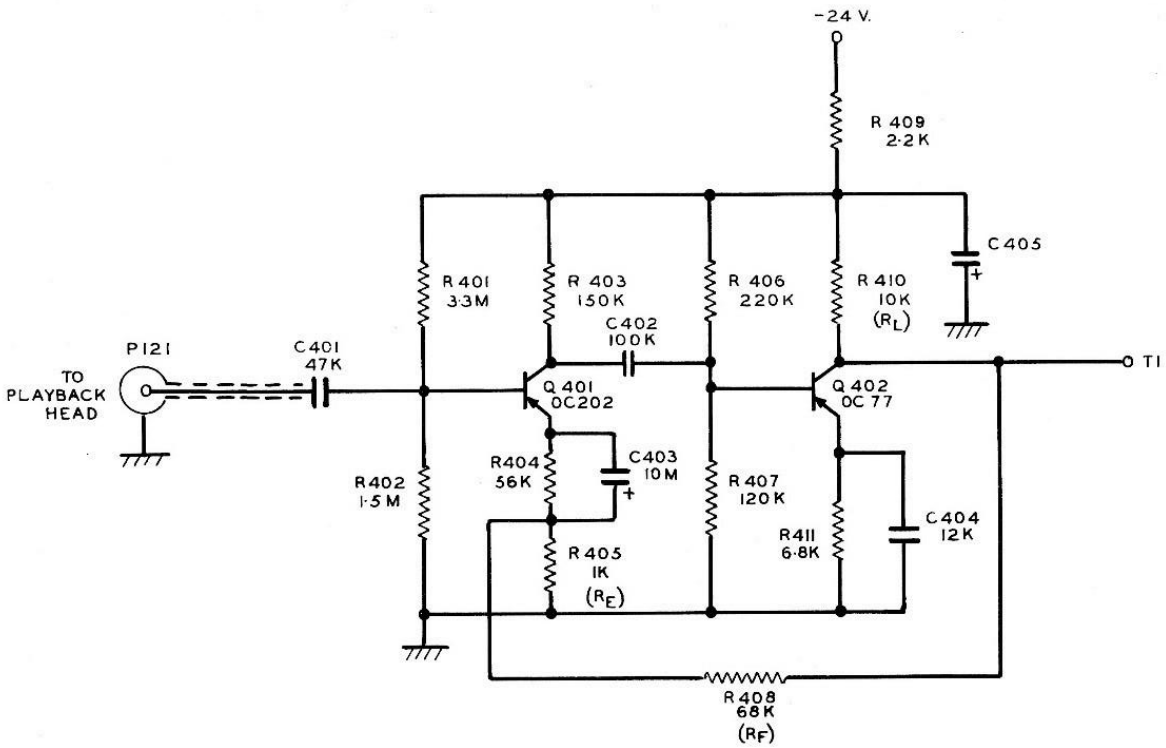


Figure 50: Playback Signal Pre-Amplifier

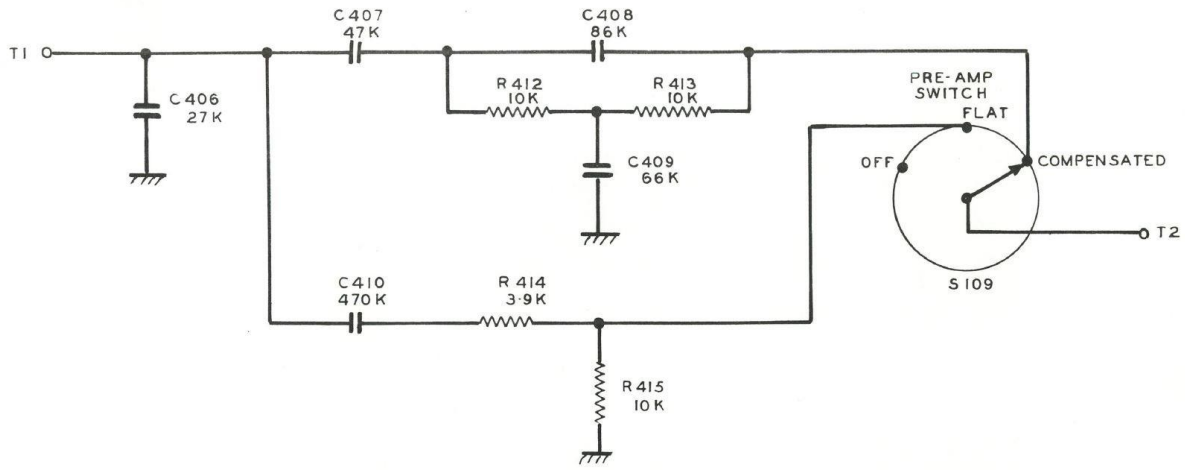


Figure 51: Compensating Network

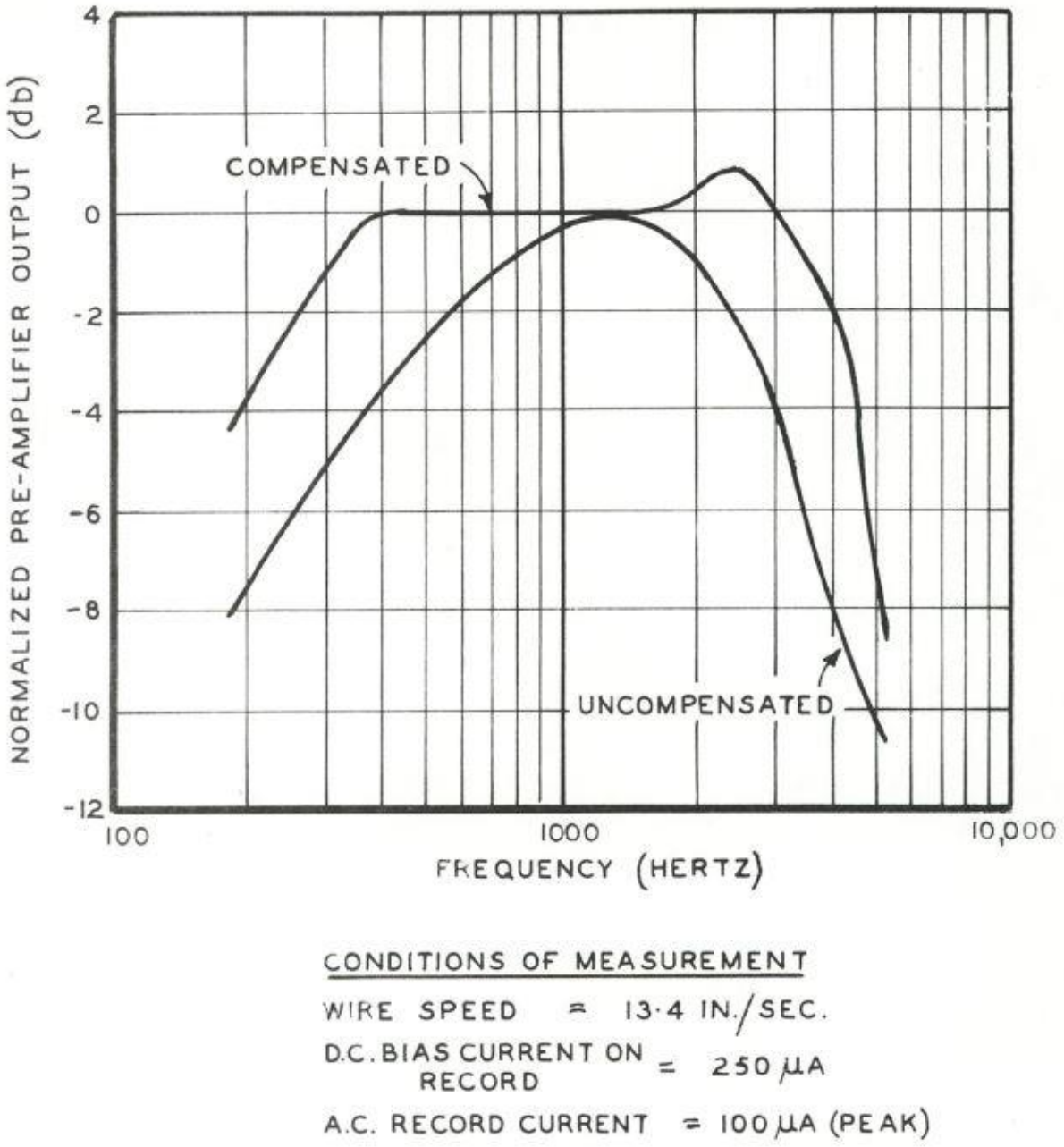


Figure 52: Comparative Responses of Compensated & Uncompensated Systems (Voltage Output from Amplifier for Constant Amplitude of Record Current)

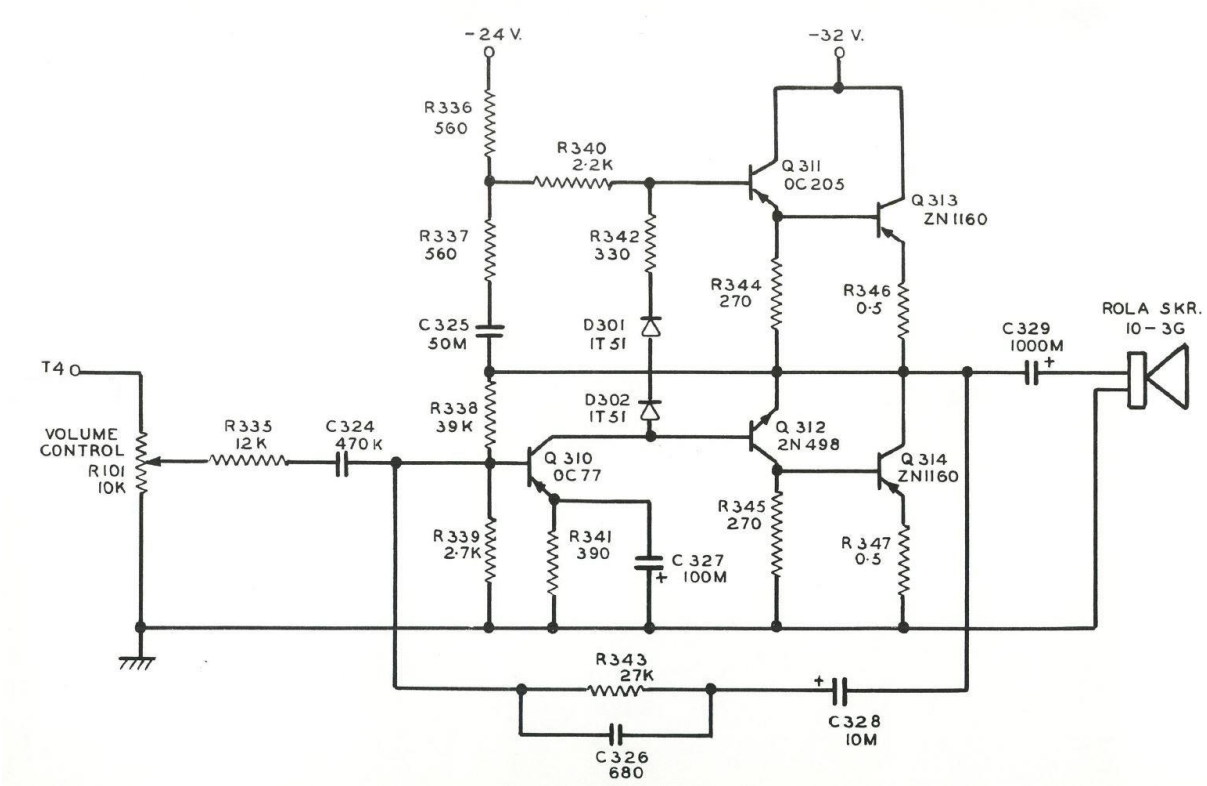


Figure 53 Cockpit Voice Power Amplifier and Speaker

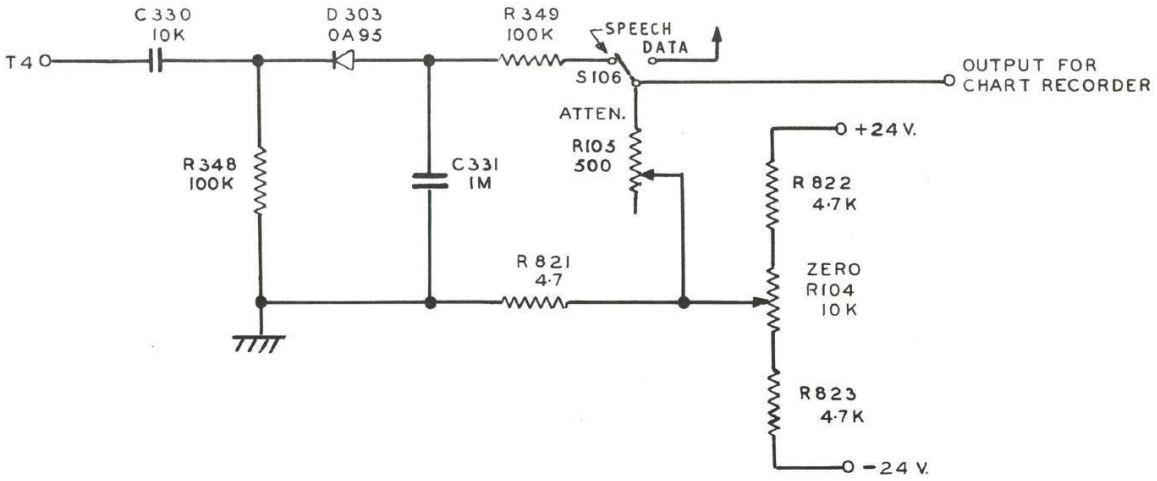


Figure 54: Cockpit Voice Voltage Level Indicator

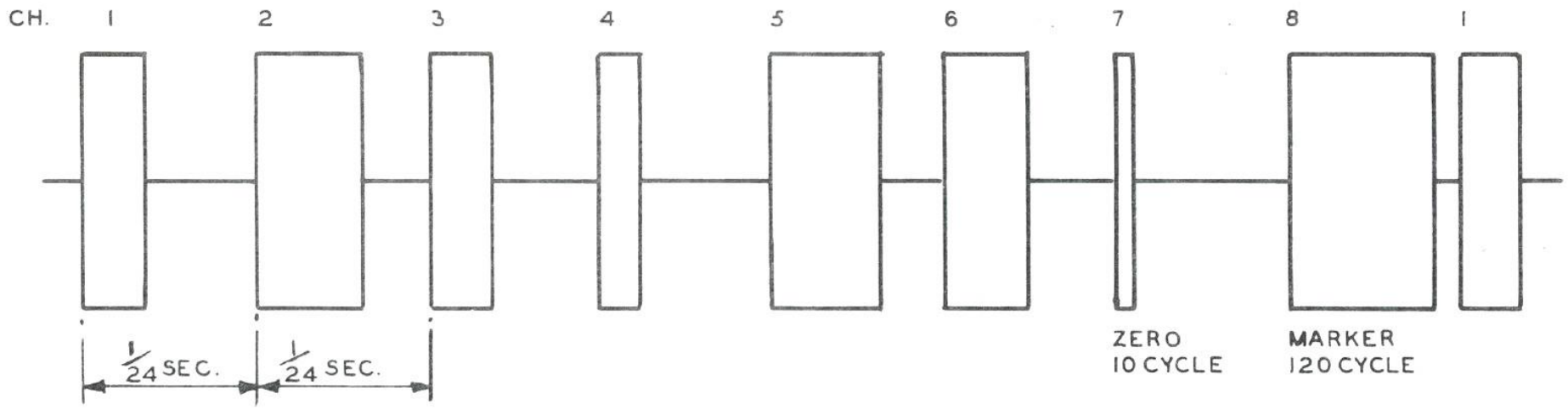


Figure 55: Envelopes of Recorded Data Signal (3500 Hz Sine-Wave Bursts)

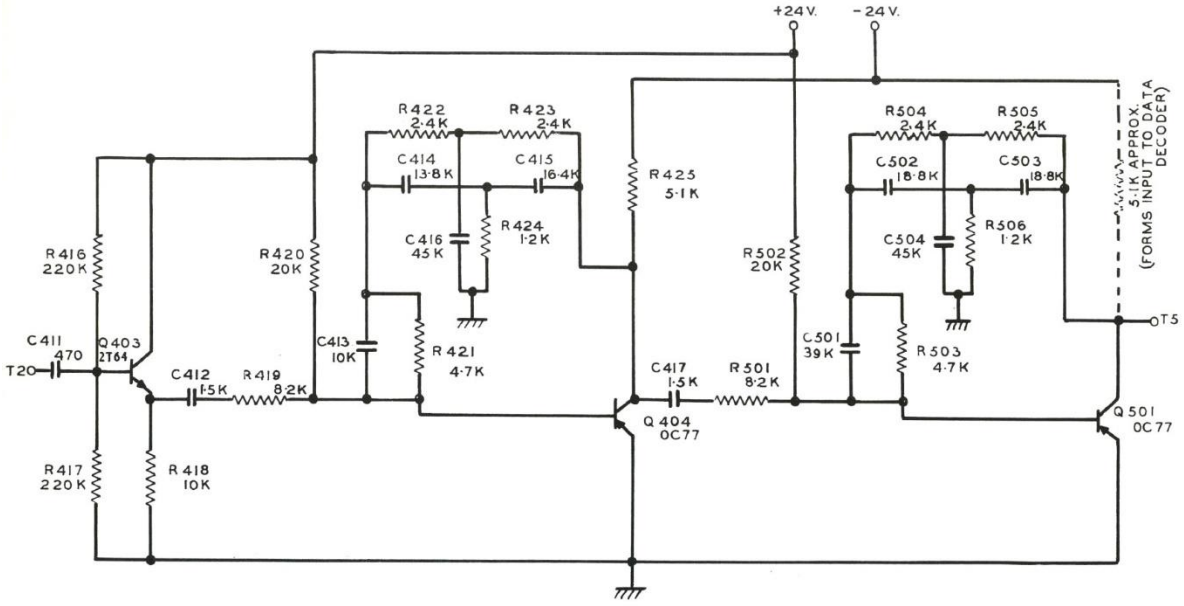


Figure 56: Flight Data Extractor (Band-Pass Filter)

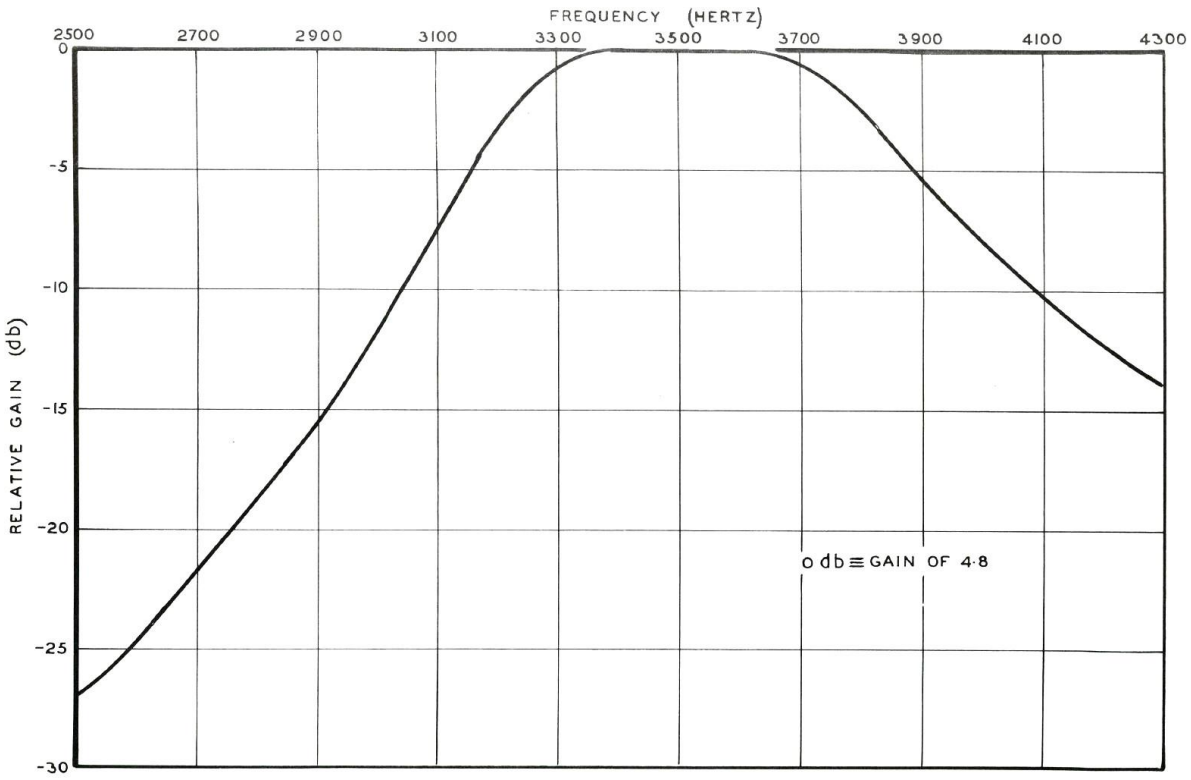


Figure 57: Frequency Response of Flight Data Band-Pass Filter

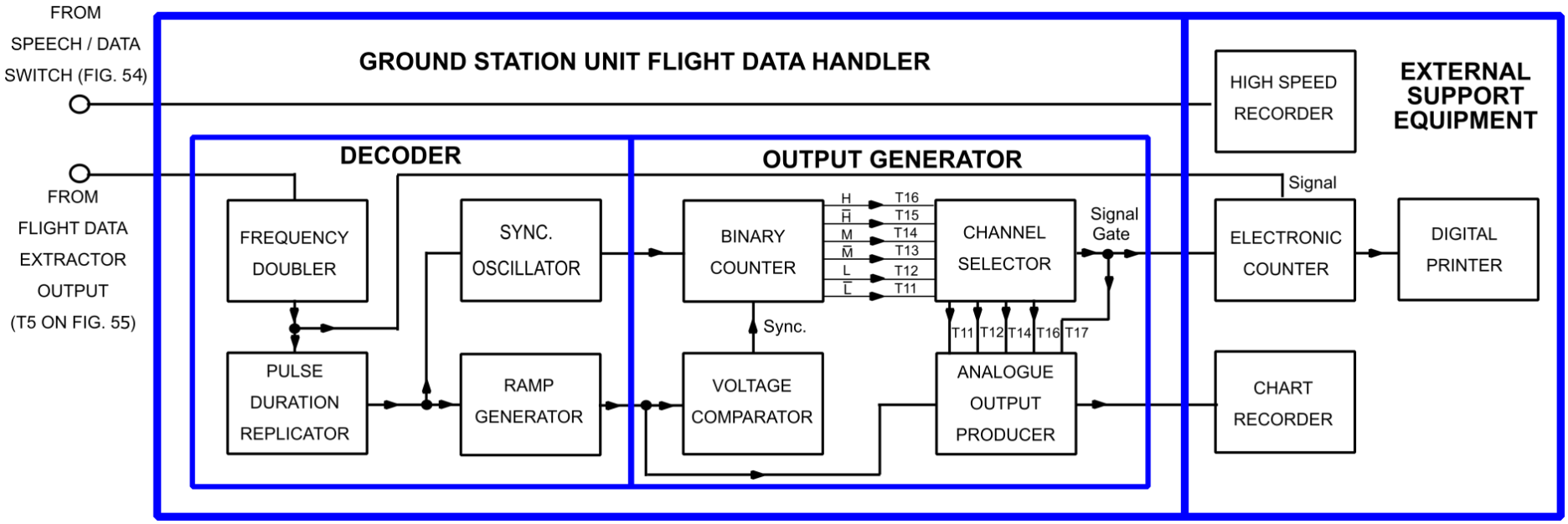


Figure 58: Block Schema of Flight Data System After Extractor

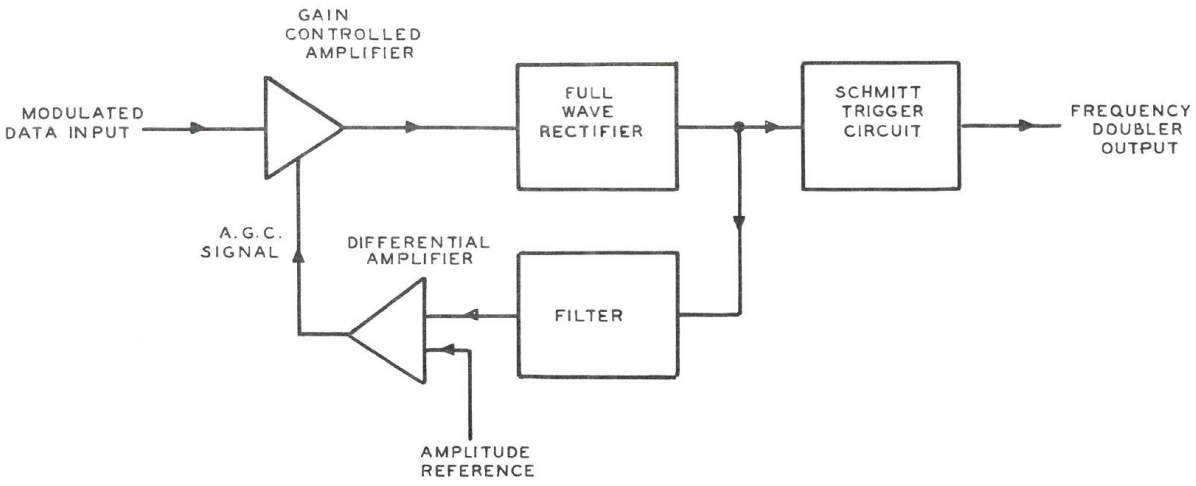


Figure 59: Frequency Doubler Block Schema

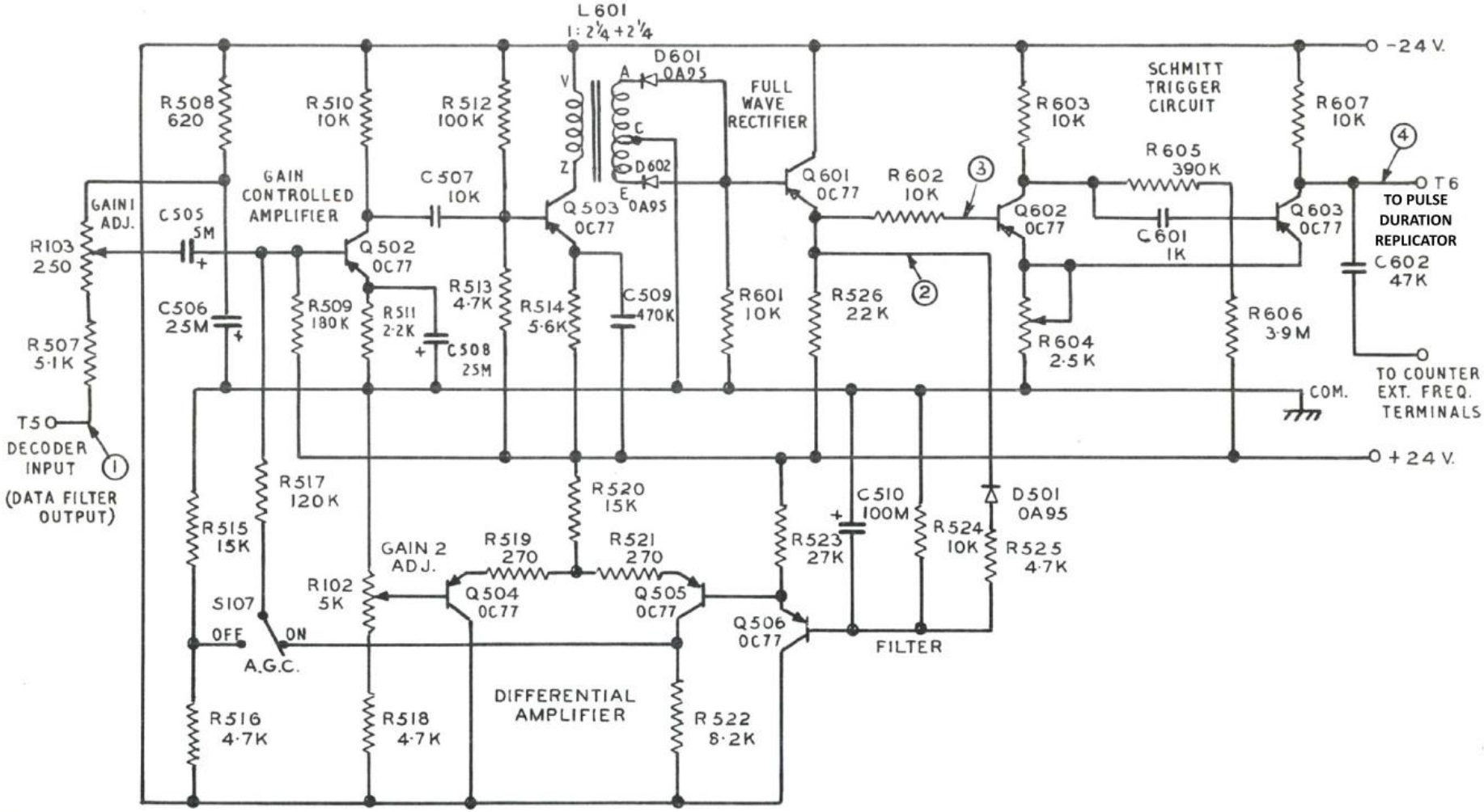


Figure 60: Frequency Doubler and Associated Schmitt Trigger Circuit

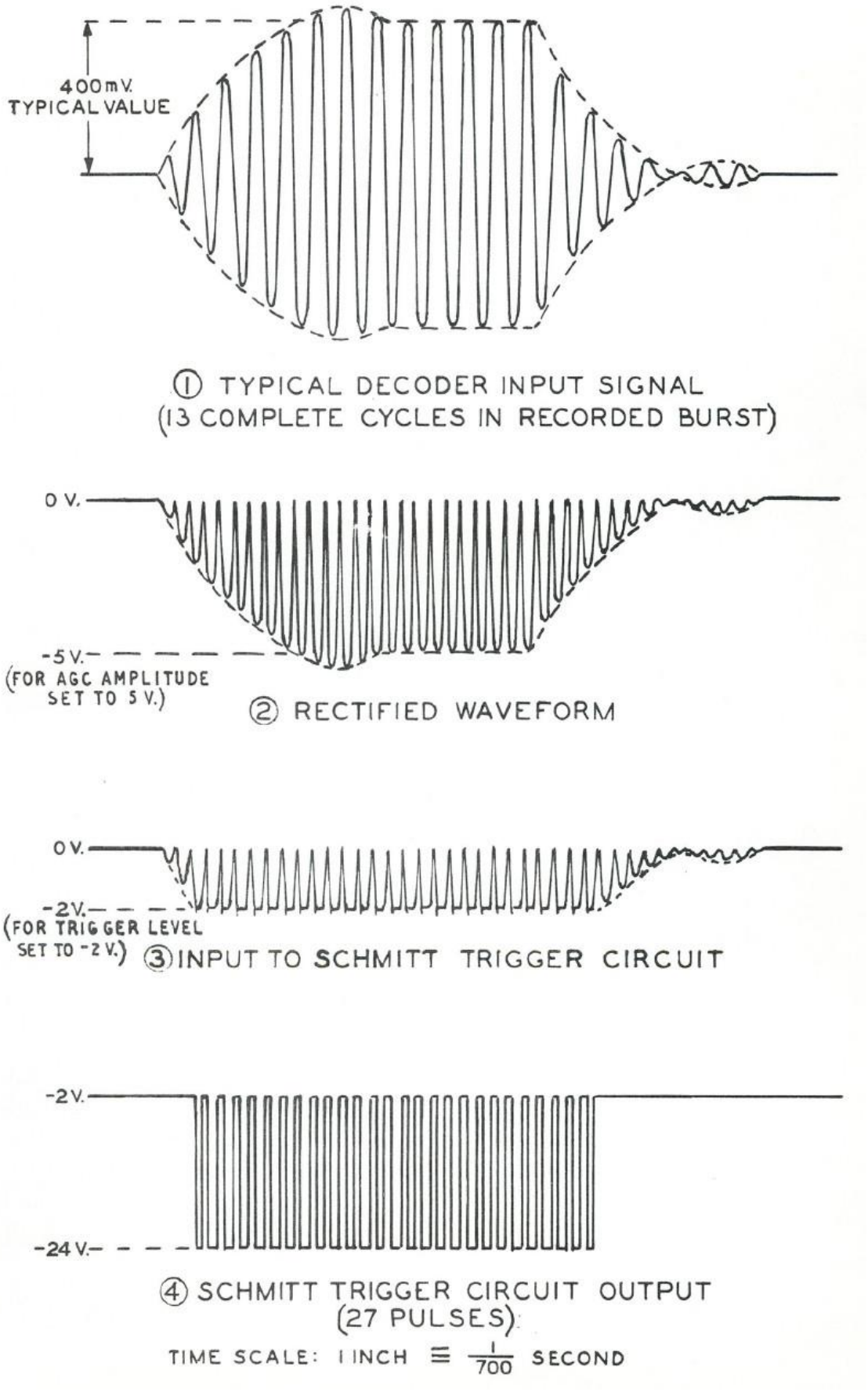
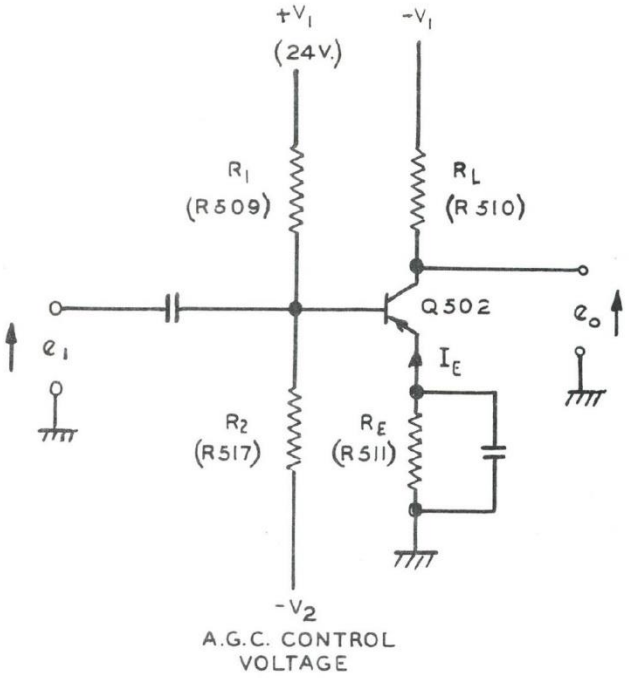


Figure 61: Waveforms Relevant to Frequency Doubler

(a) Actual Circuit



(b) Small Signal Equivalent Circuit

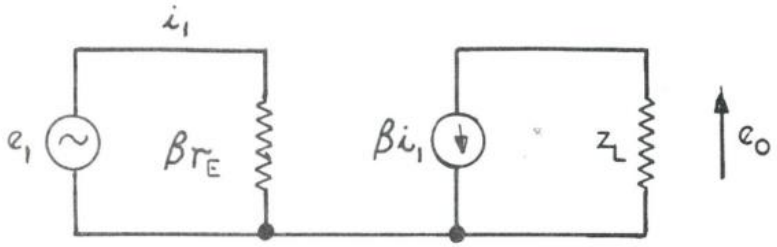


Figure 62: Gain Controlled Amplifier

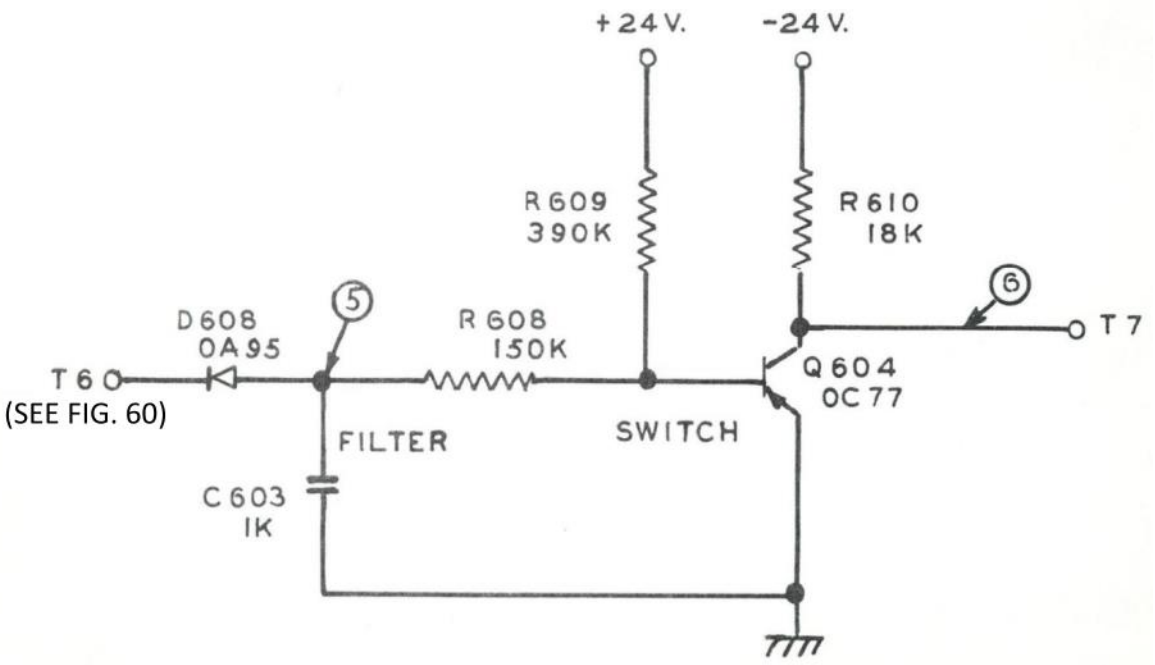


Figure 63: Pulse Duration Replicator

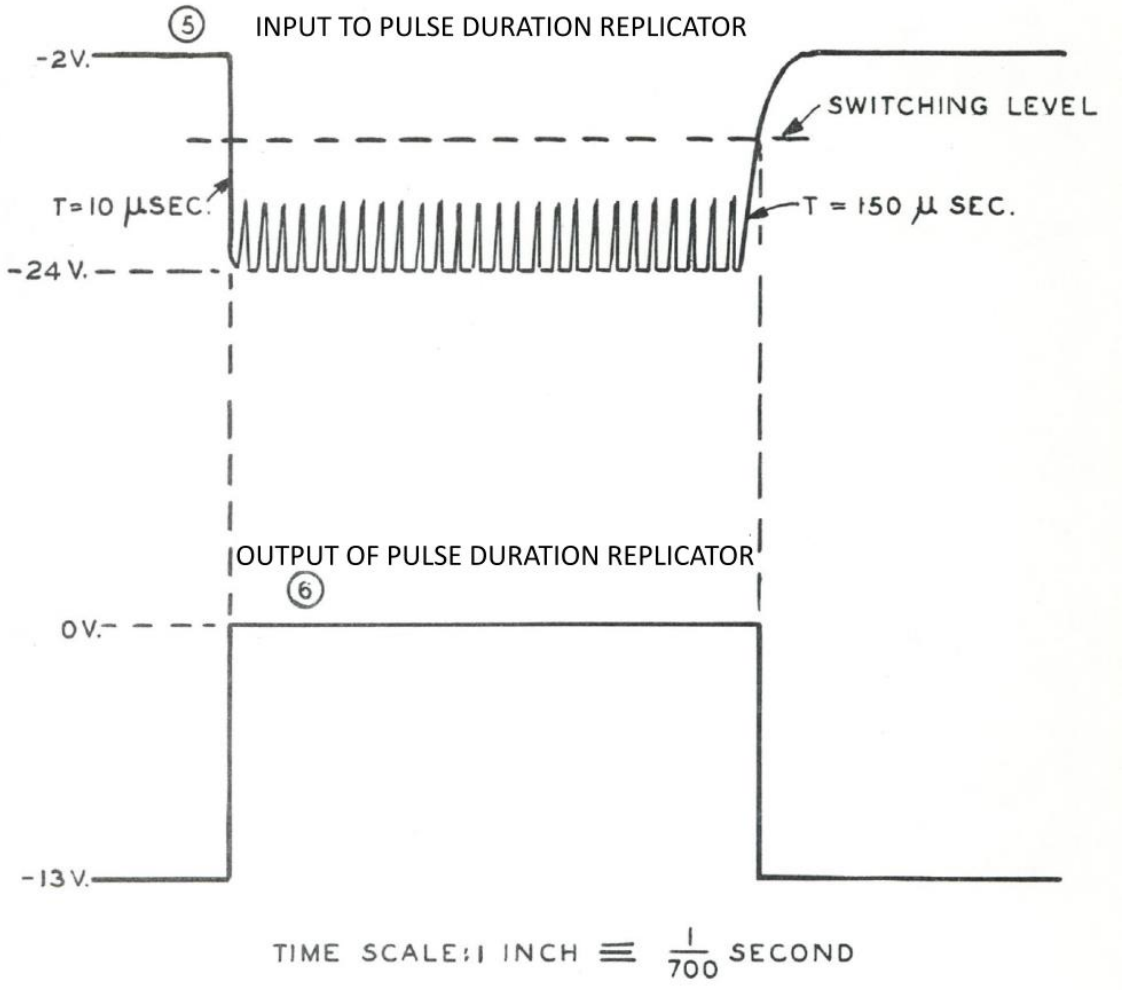


Figure 64: Waveforms Relevant to Pulse Duration Replicator

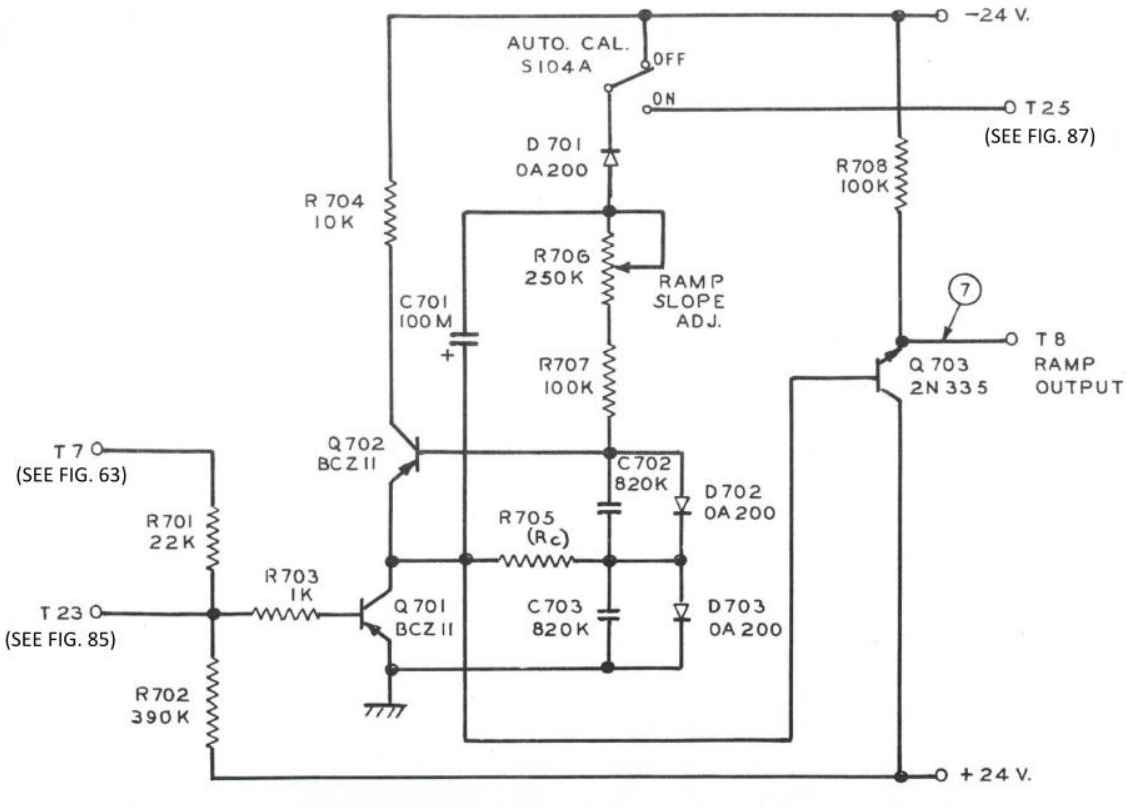
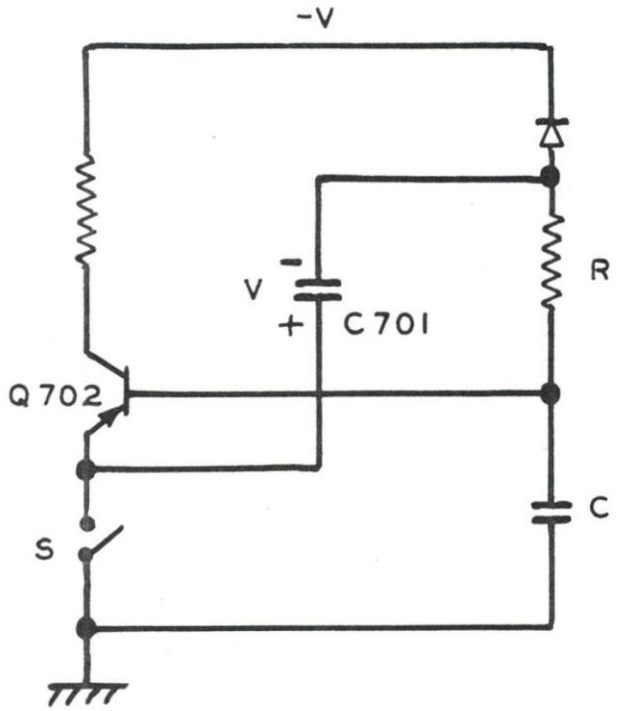


Figure 65: Ramp Generator Final Circuit

(a) Conventional Circuit



(b) Compensated Circuit

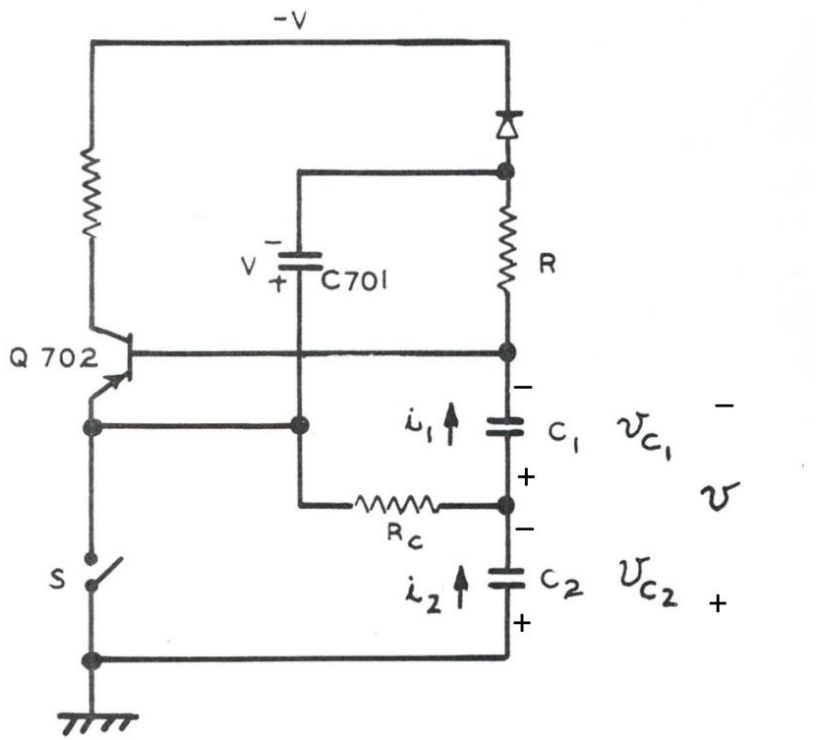


Figure 66: Comparison of Conventional and Compensated Ramp Circuits

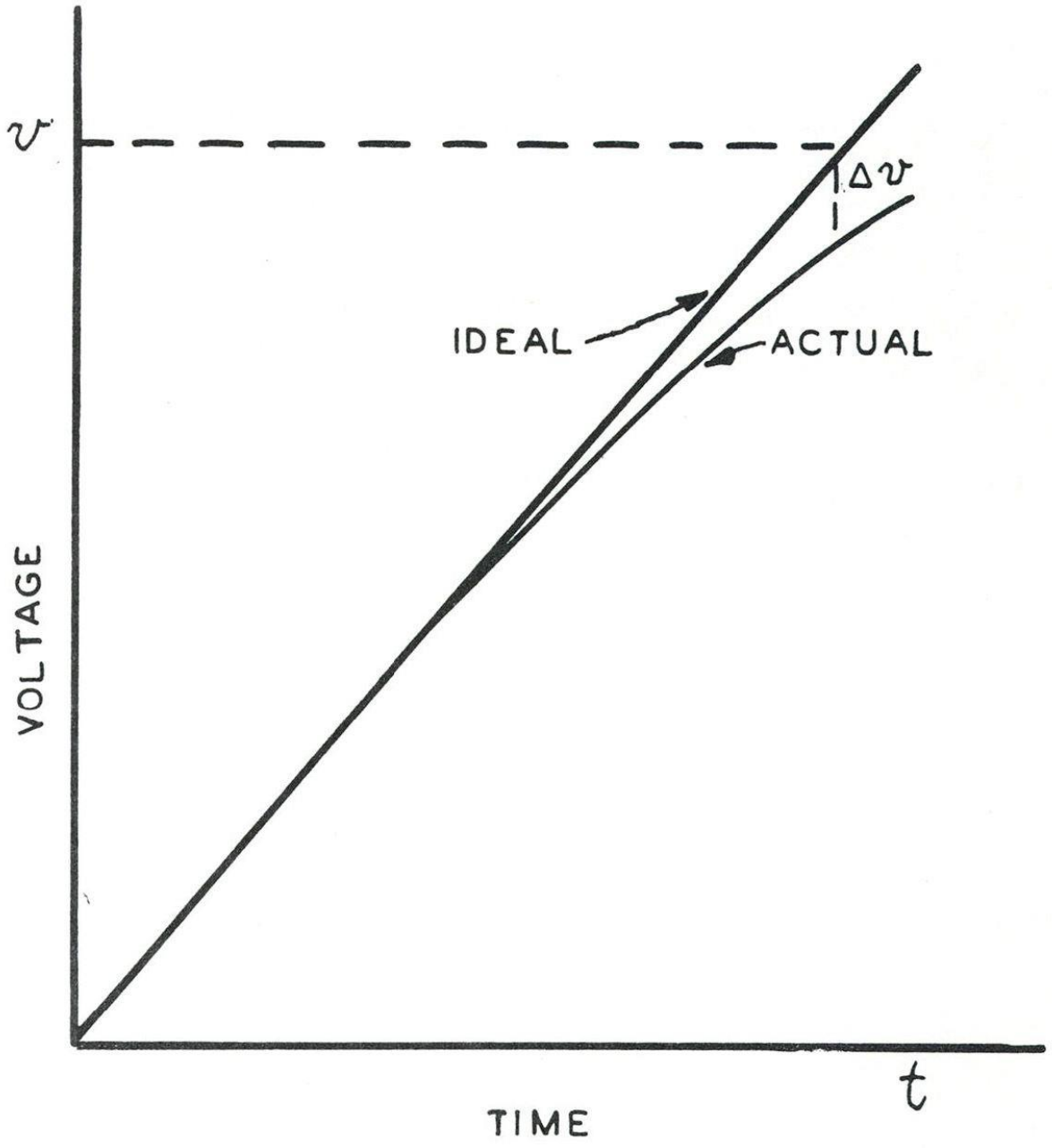


Figure 67: Curve Showing Departure of Ramp from a Linear Path

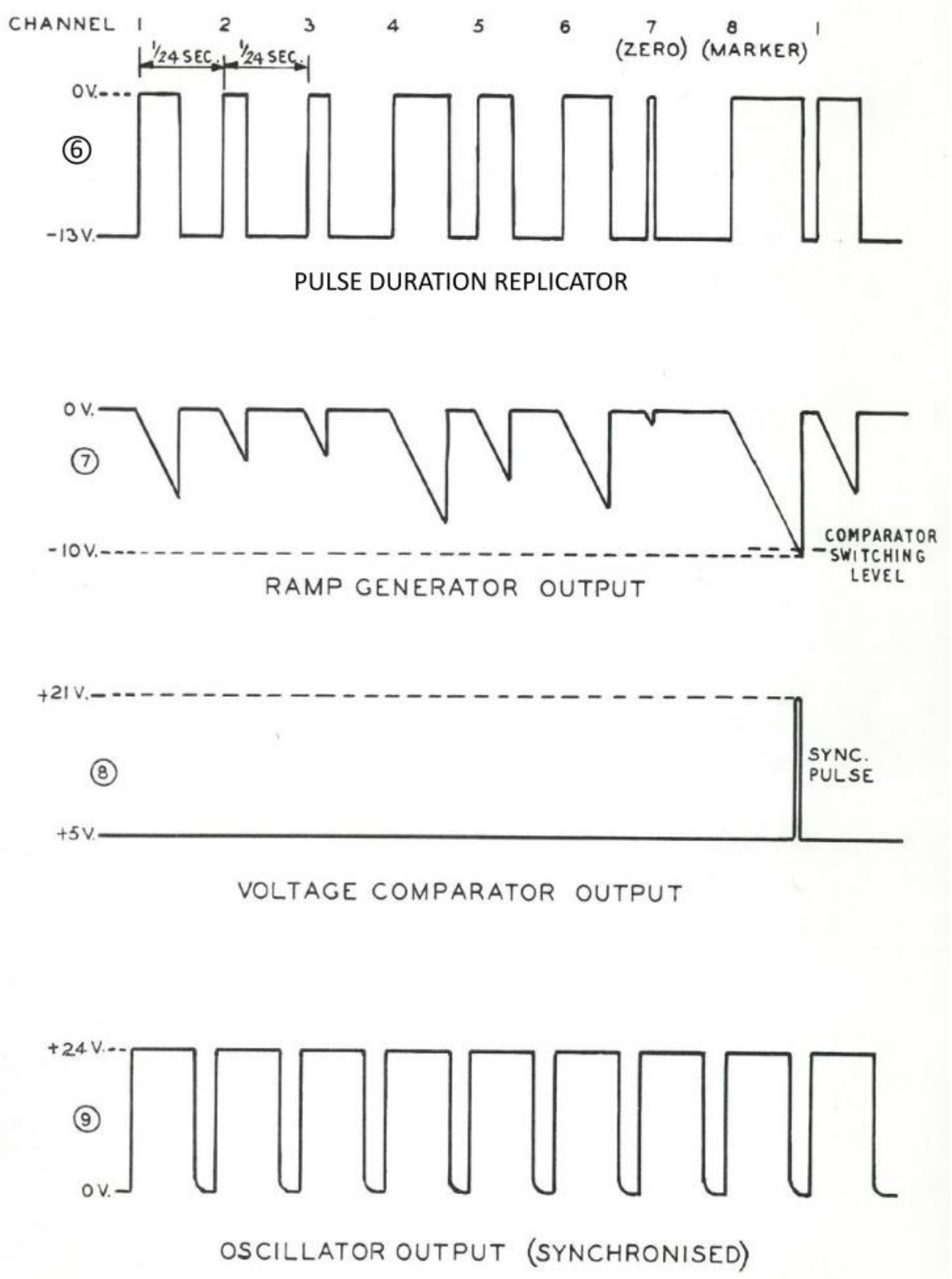


Figure 68: Waveforms Relevant to Ramp Generator, Voltage Comparator and Oscillator

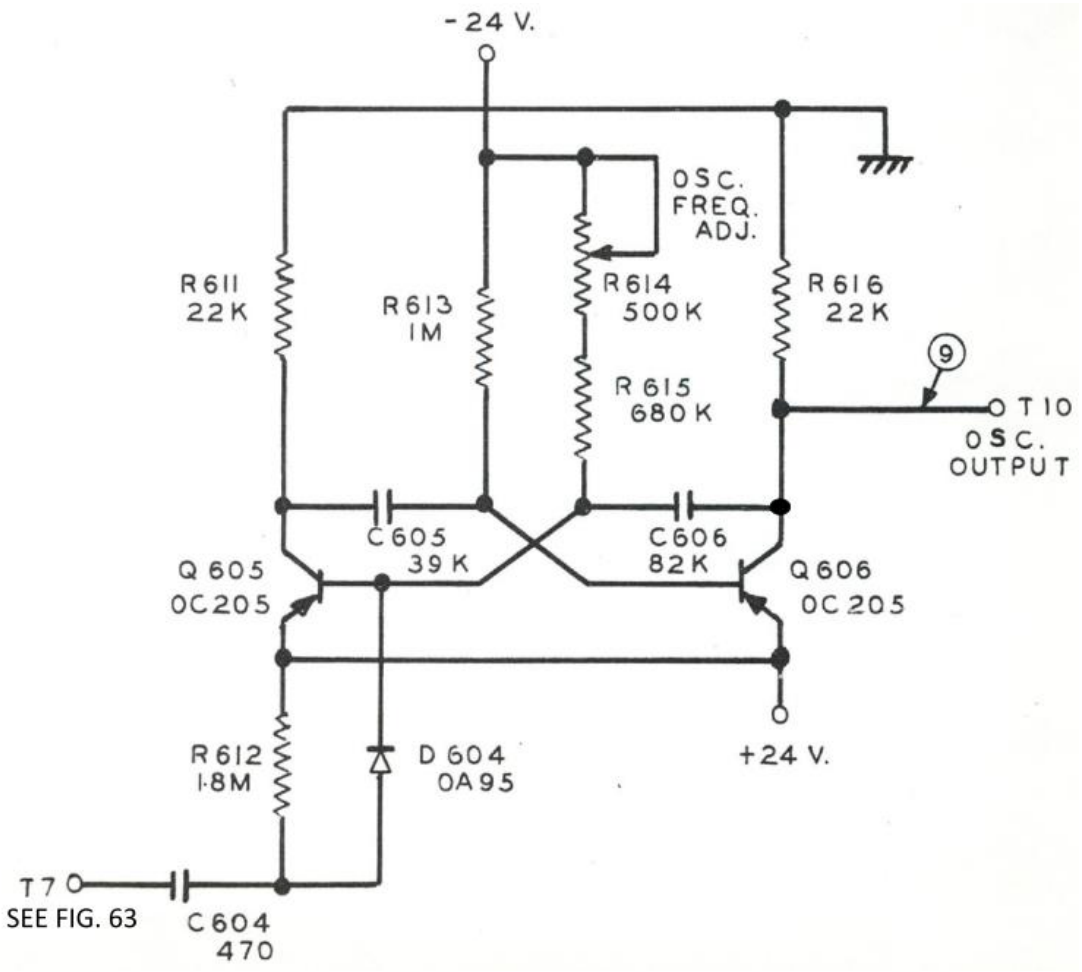
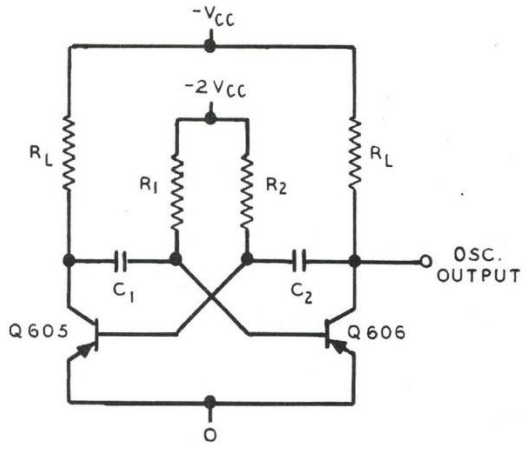
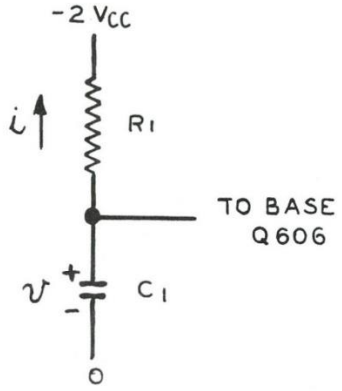


Figure 69: Synchronised Oscillator

(a) Basic Oscillator Circuit



(b) Equivalent Discharge Circuit for C_1



(c) Oscillator Output Waveform

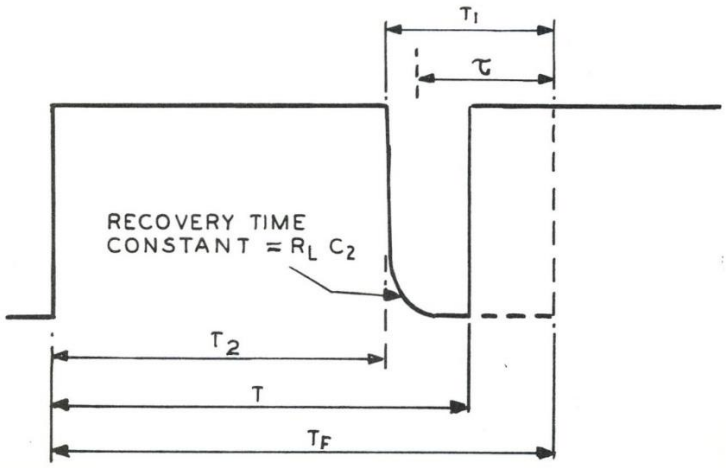


Figure 70: Basic Diagrams Supporting Oscillator Analysis

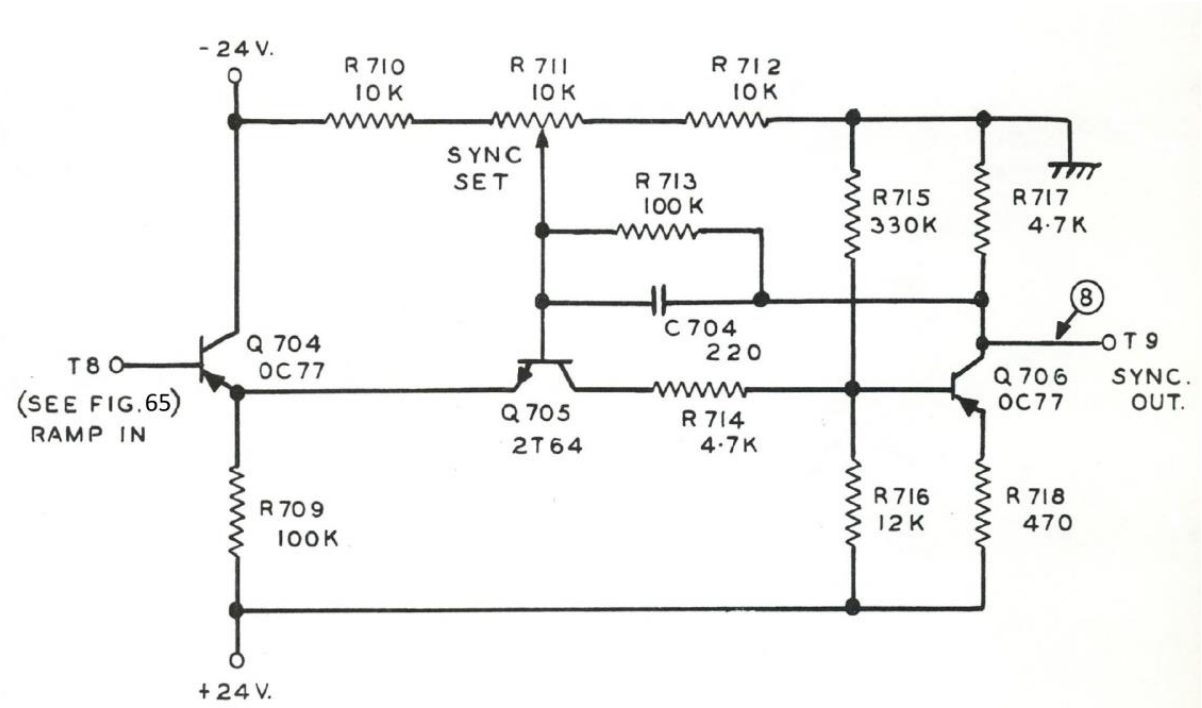


Figure 71: Voltage Comparator

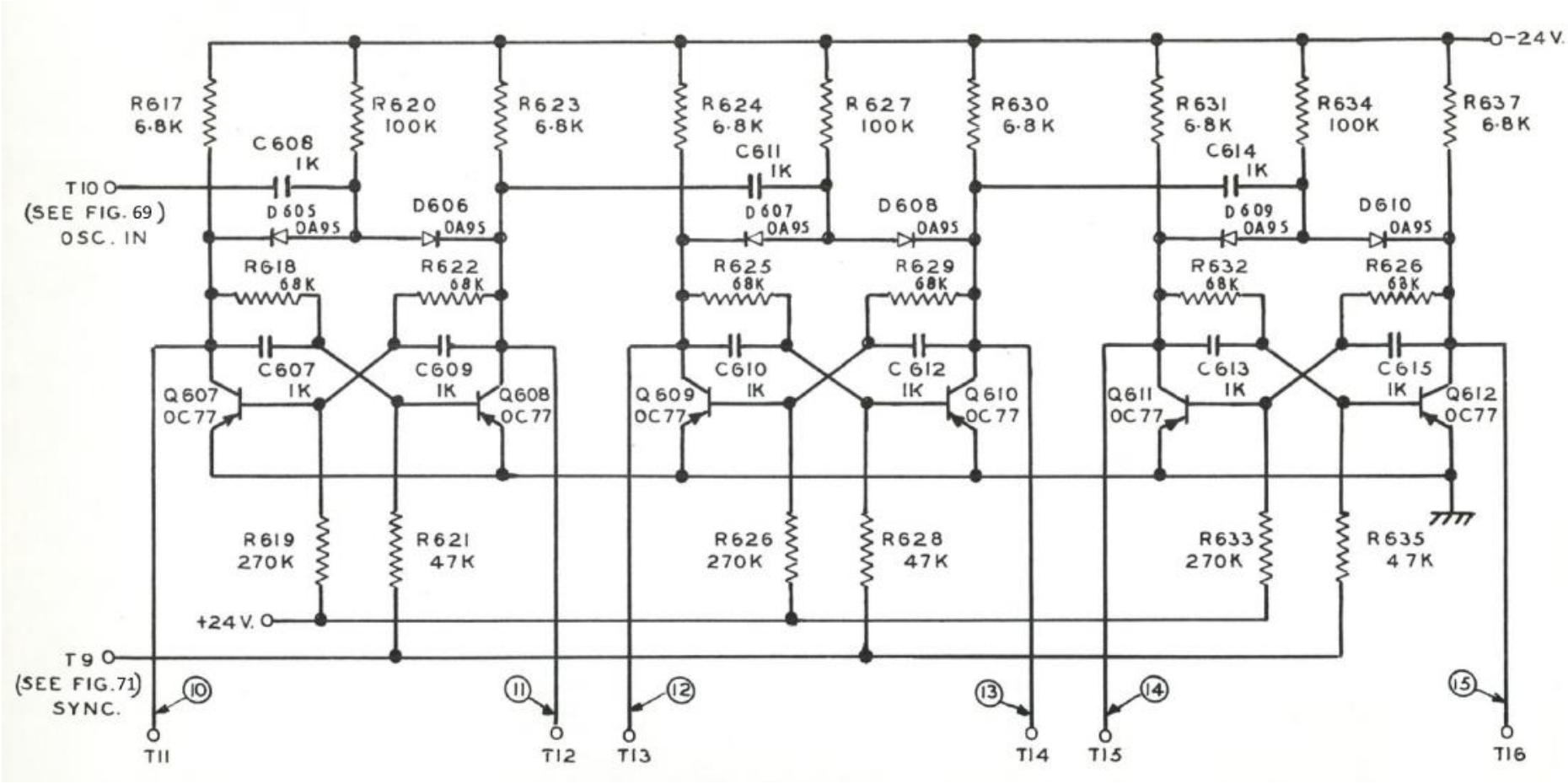


Figure 72: Binary Counter (Divide by 8)

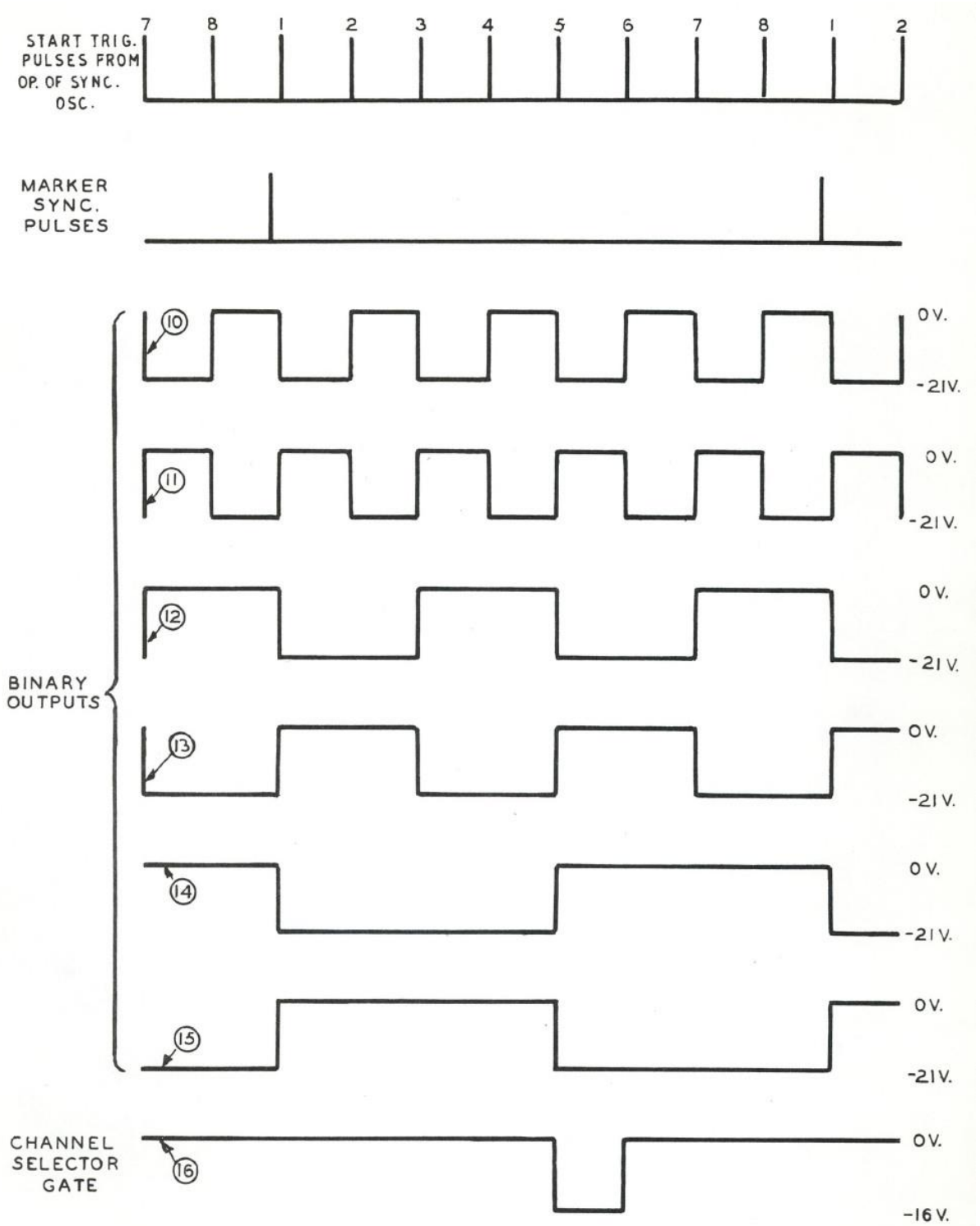
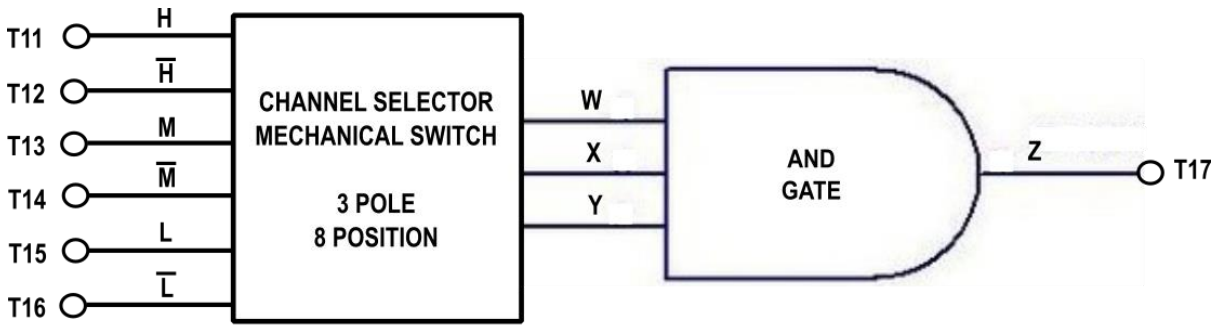


Figure 73: Waveforms Relevant to Binary Counter and Channel Selector



TRUTH TABLE

INPUTS			OUTPUT
W	X	Y	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Figure 74: Channel Selector Block Schema

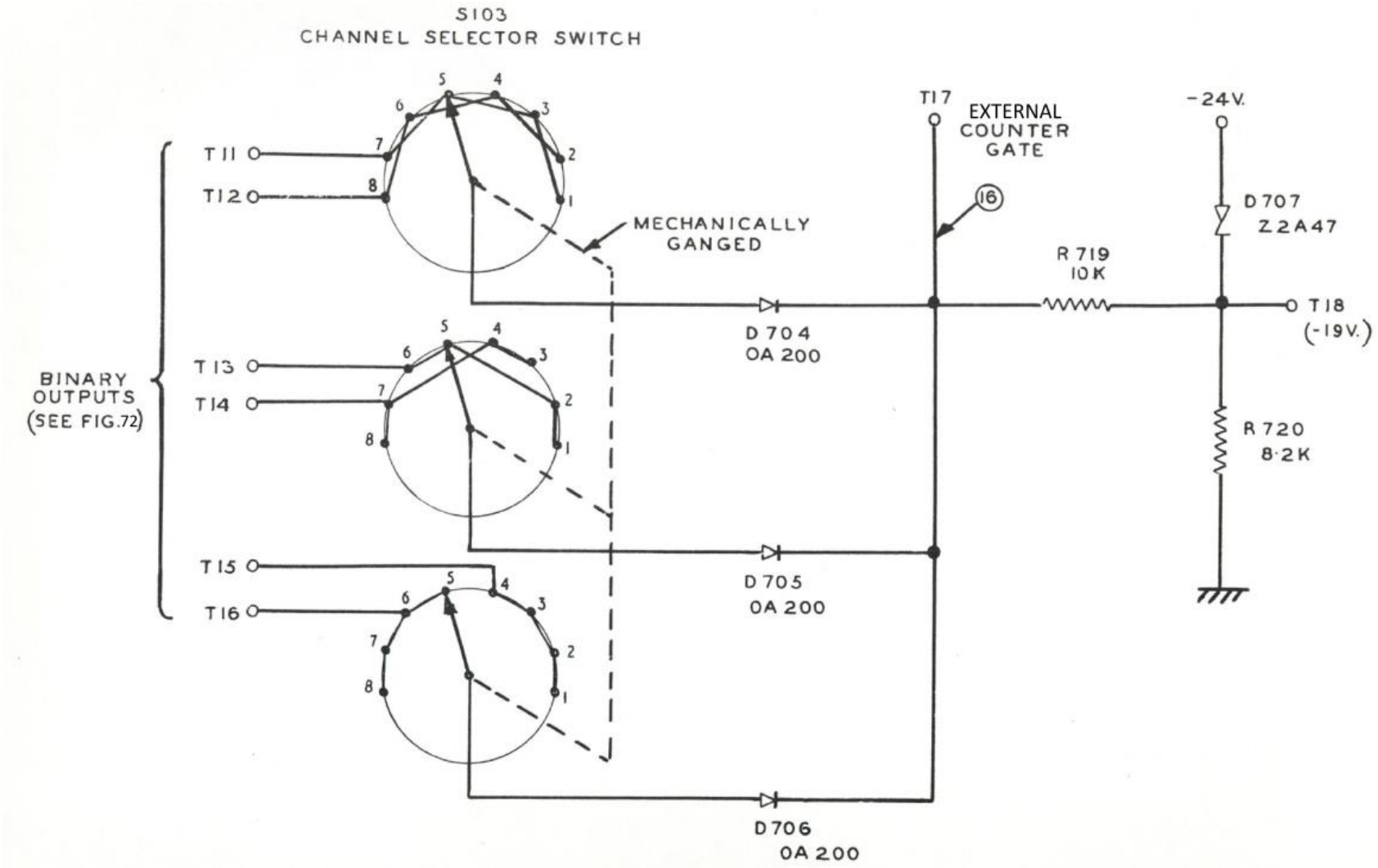


Figure 75: Channel Selector

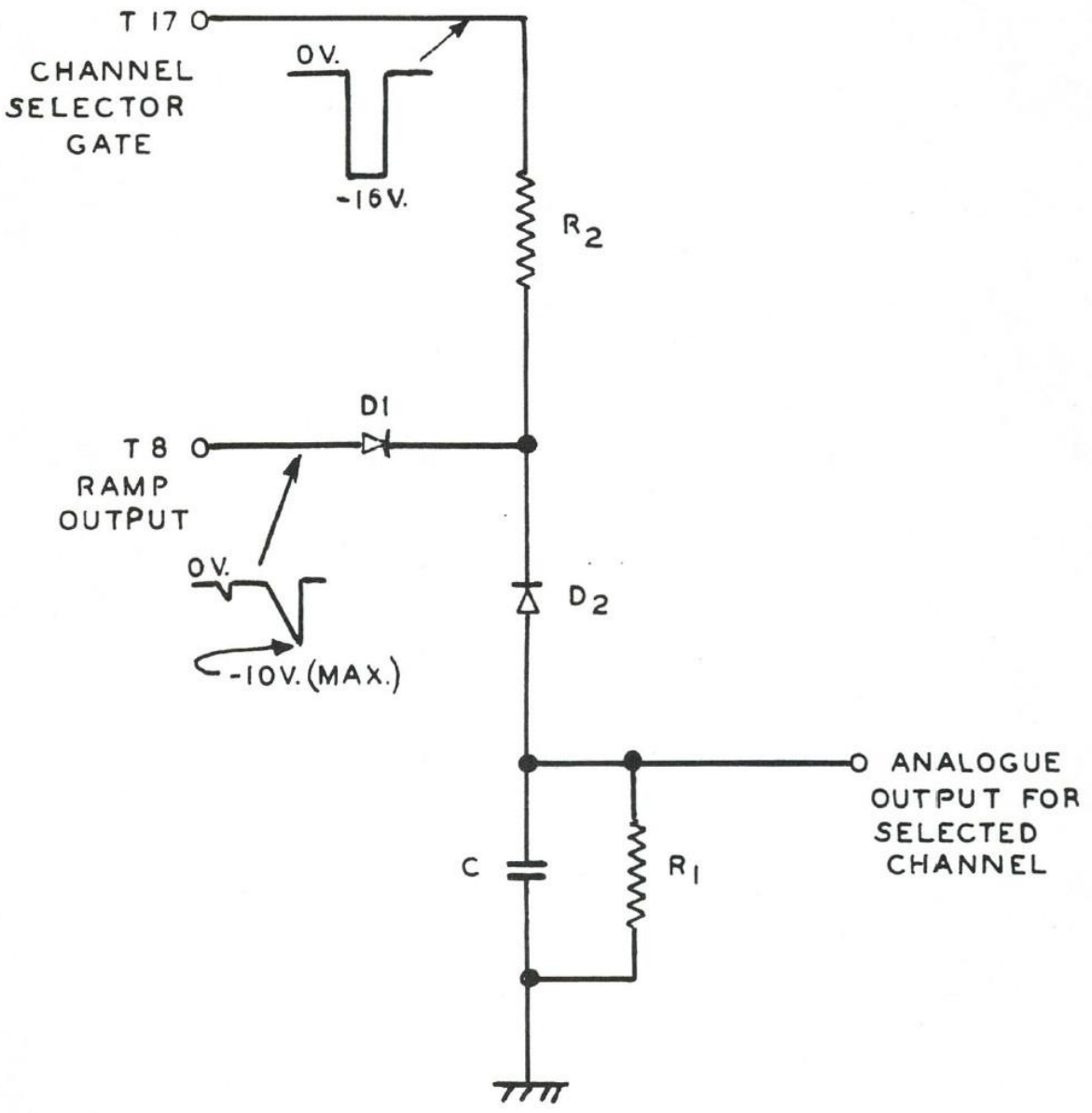


Figure 76: Simple Circuit for Single Channel Analogue Voltage Output

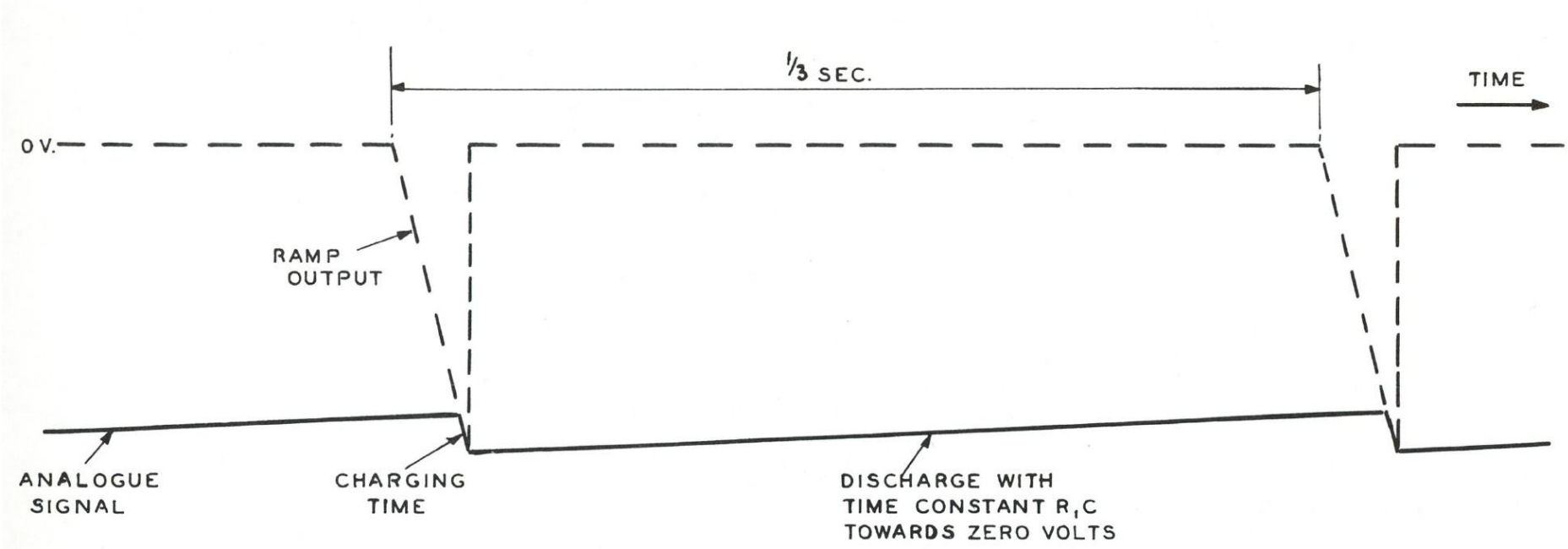


Figure 77: Output for Simple Analogue Voltage Circuit

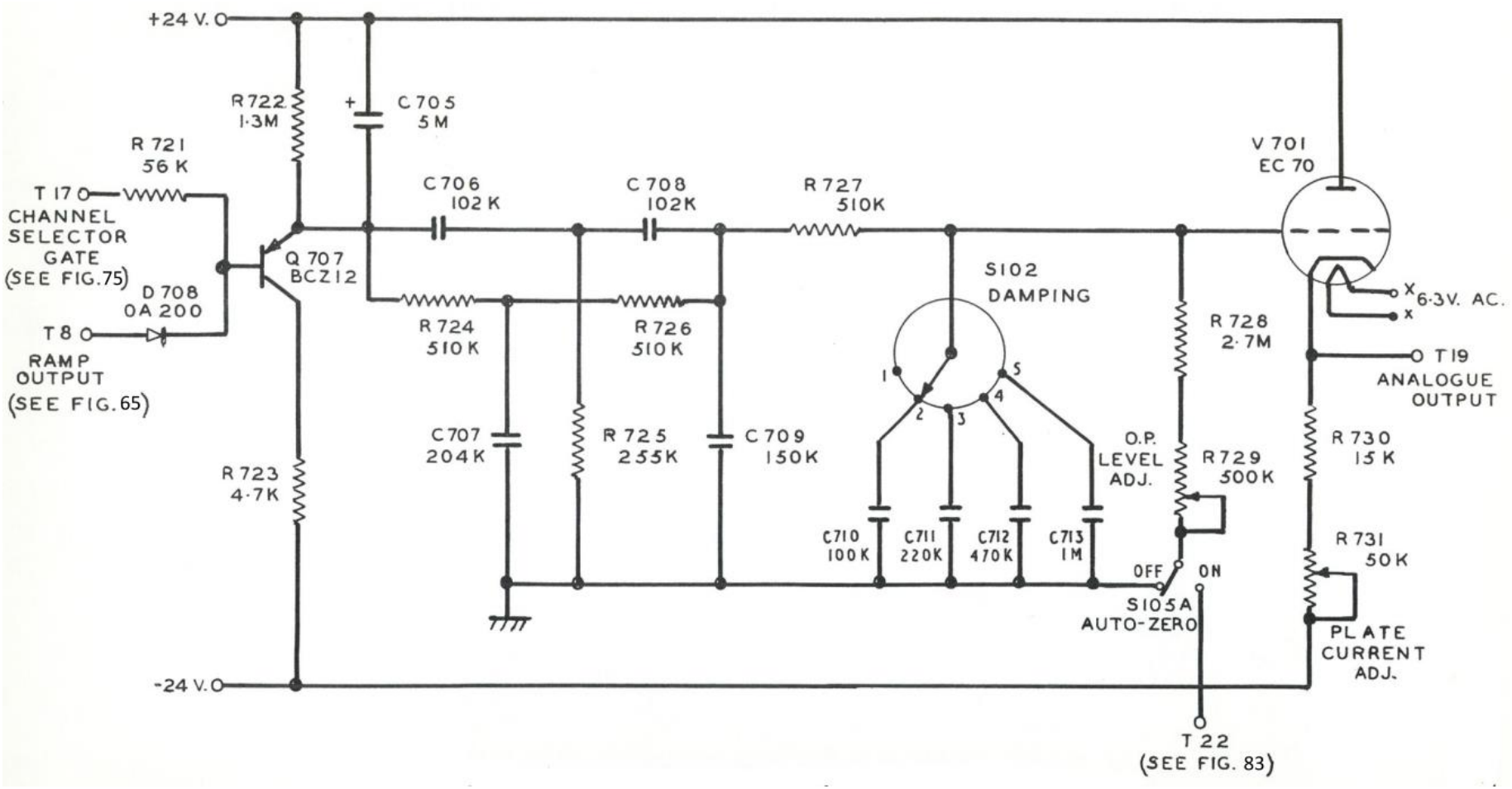


Figure 78: Signal Channel Analogue Output Voltage Generator

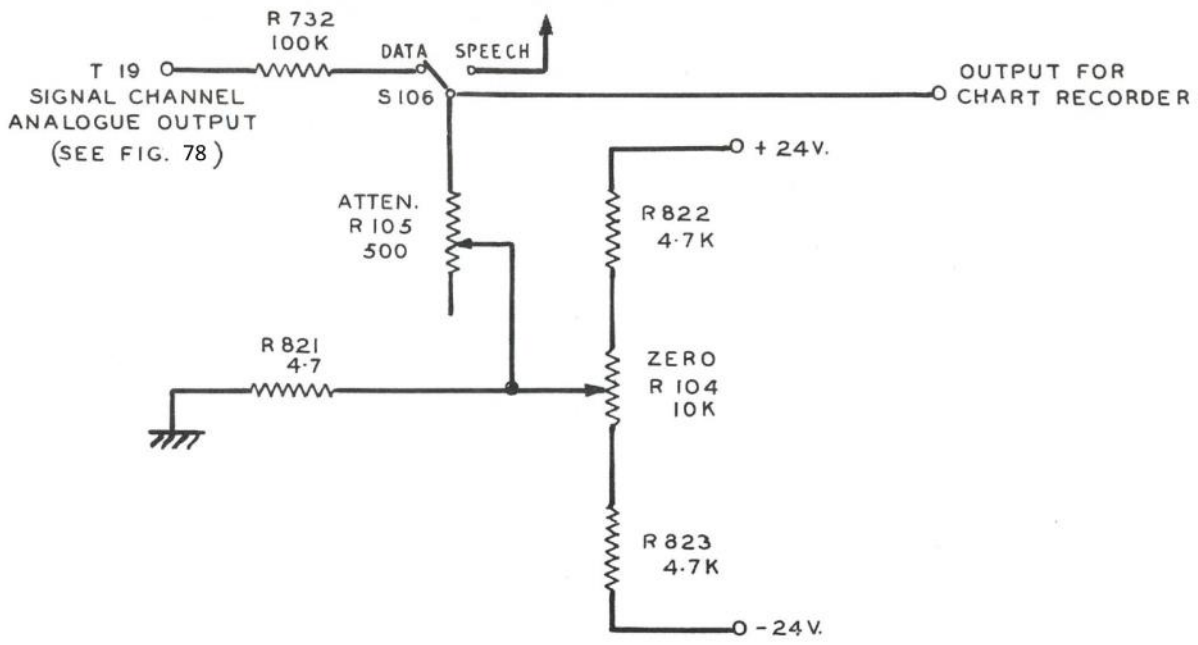


Figure 79: Analogue Output for External Chart Recorder (10 mV full scale)

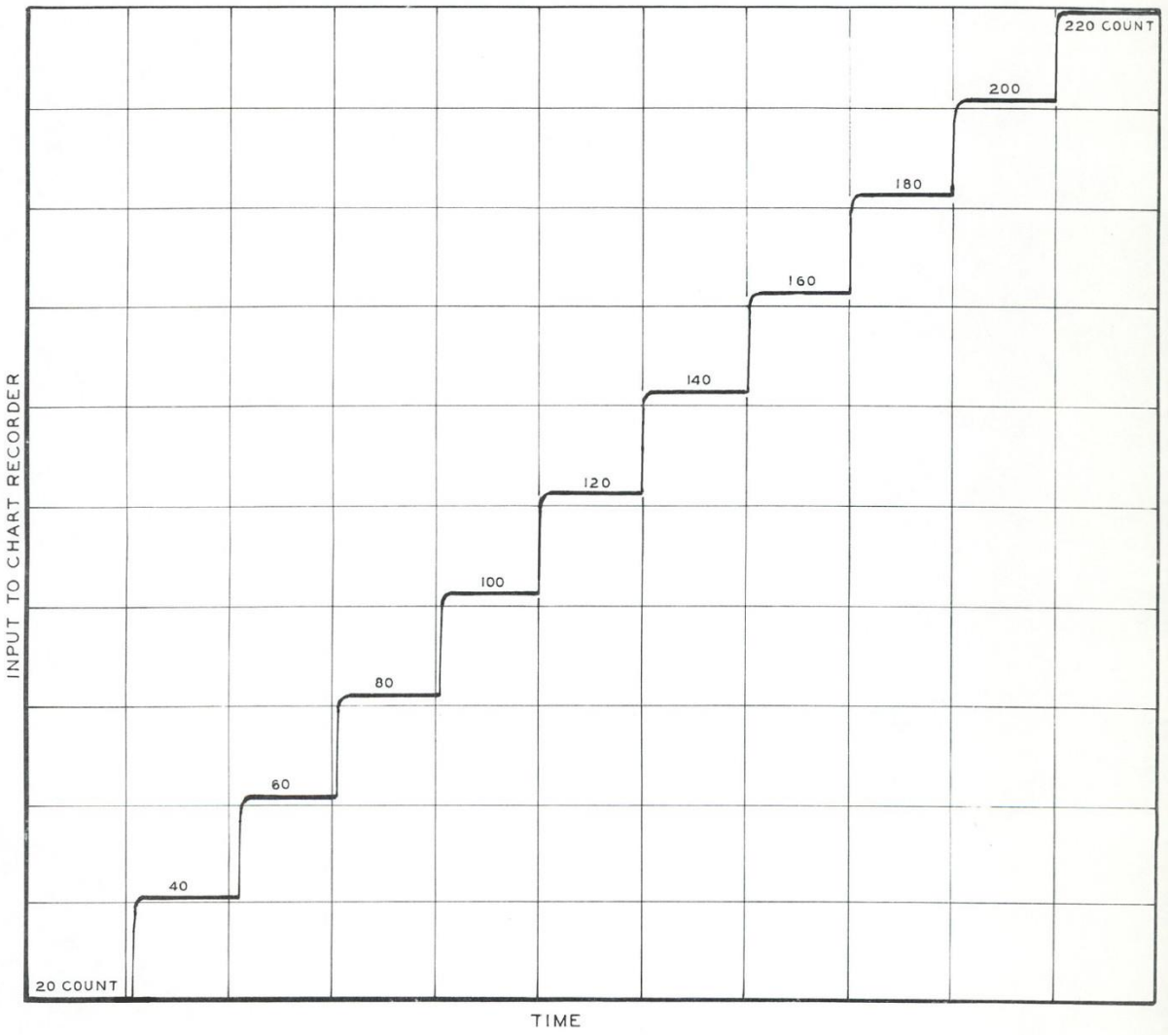


Figure 80: Analogue Circuit Linearity Measurement

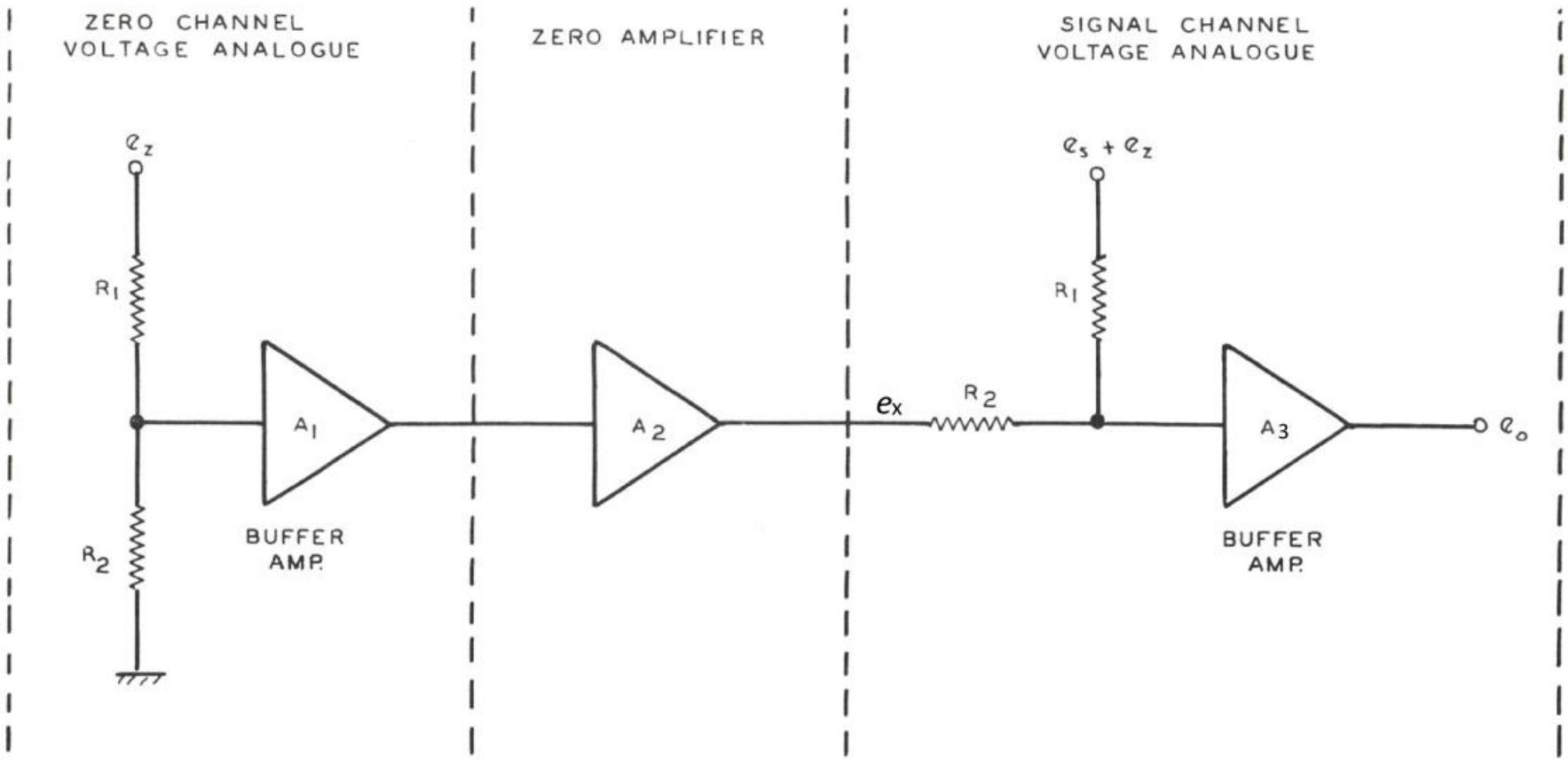


Figure 81: System of Automatic Zeroing

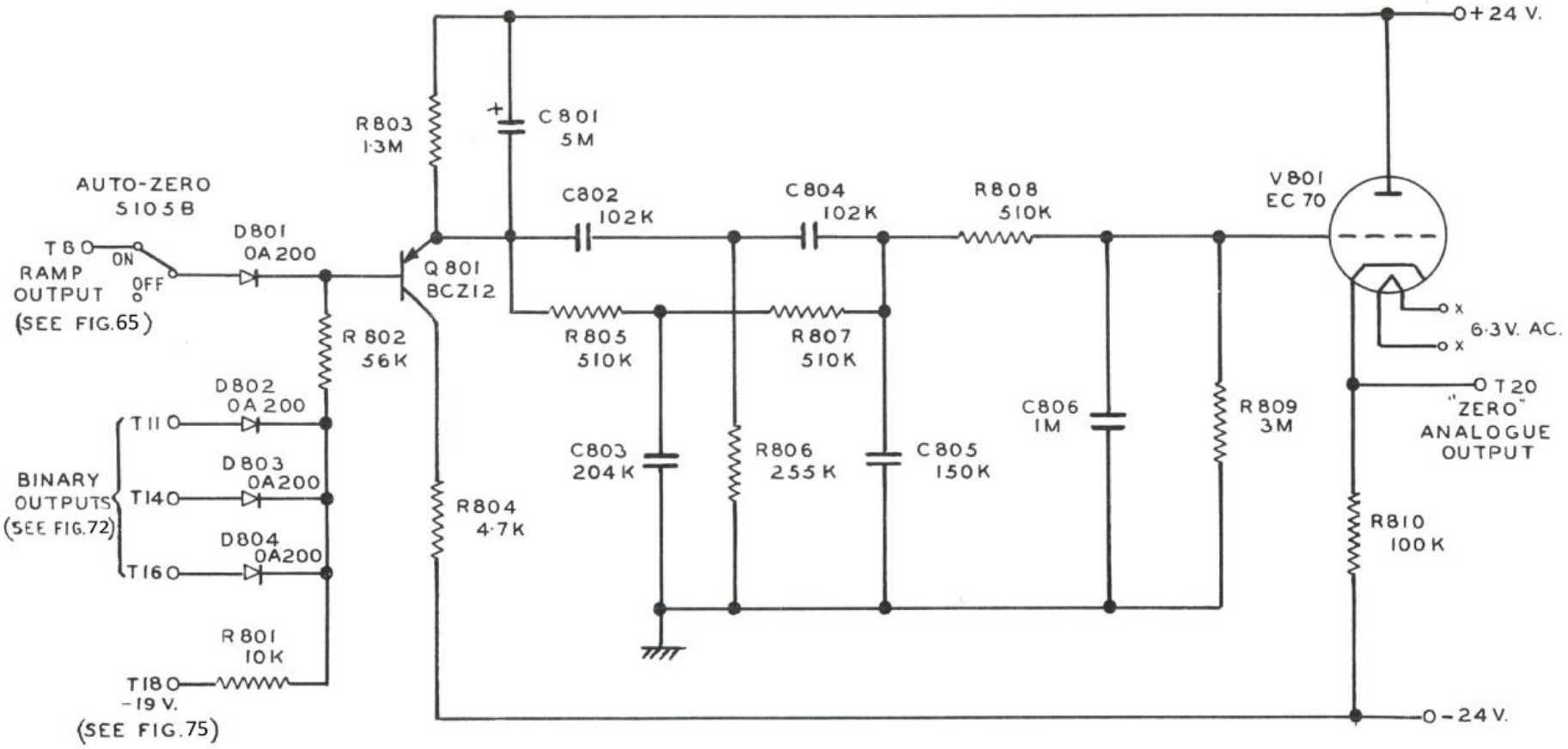


Figure 82: "Zero" Channel Analogue Output Voltage Generator

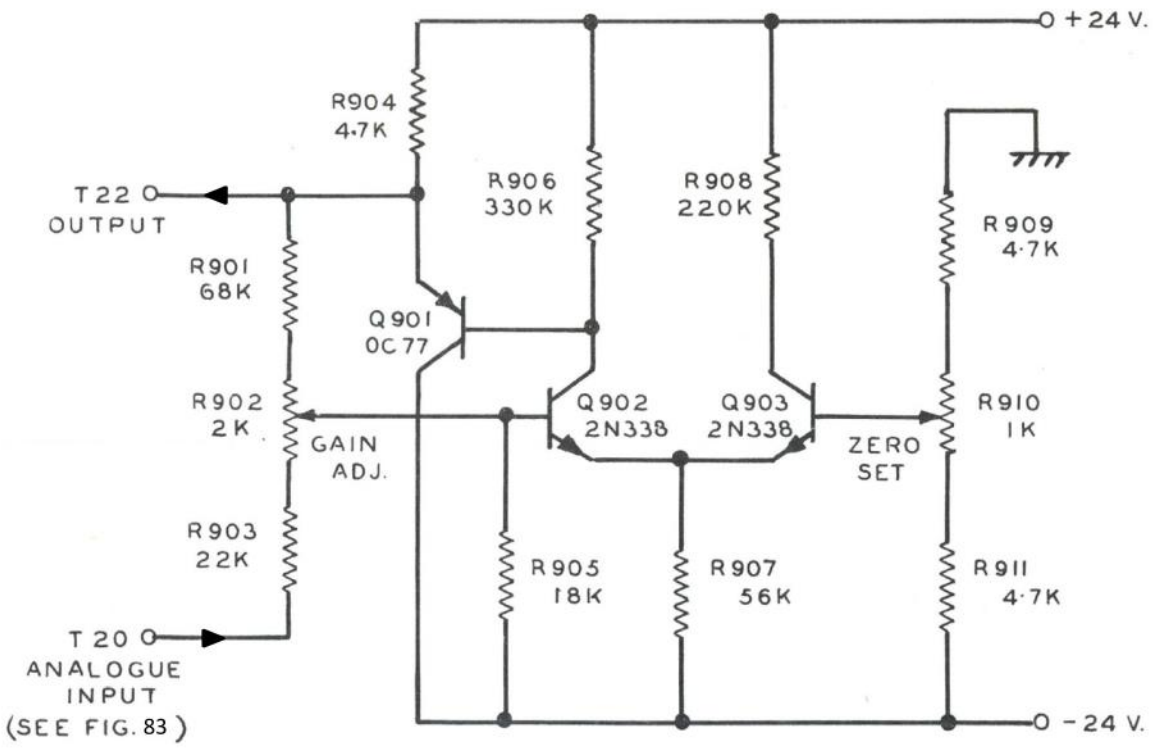


Figure 83: "Zero" Amplifier

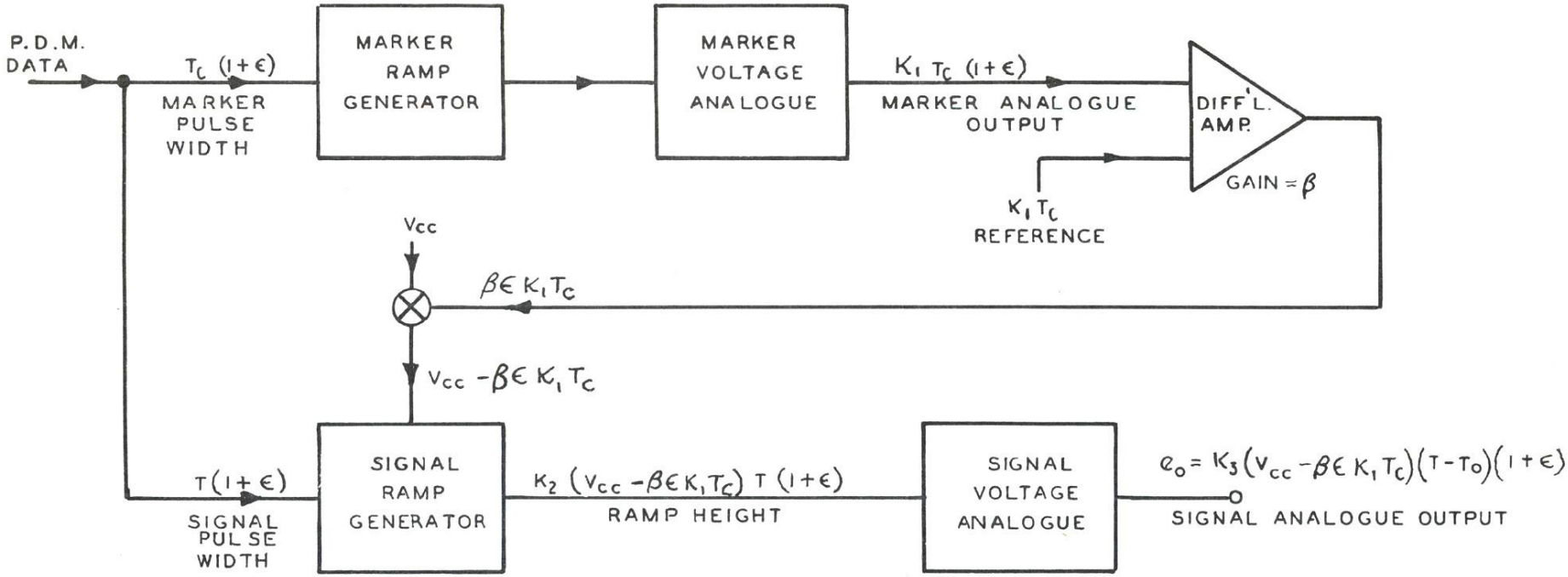


Figure 84: Automatic Calibrating System Block Schema

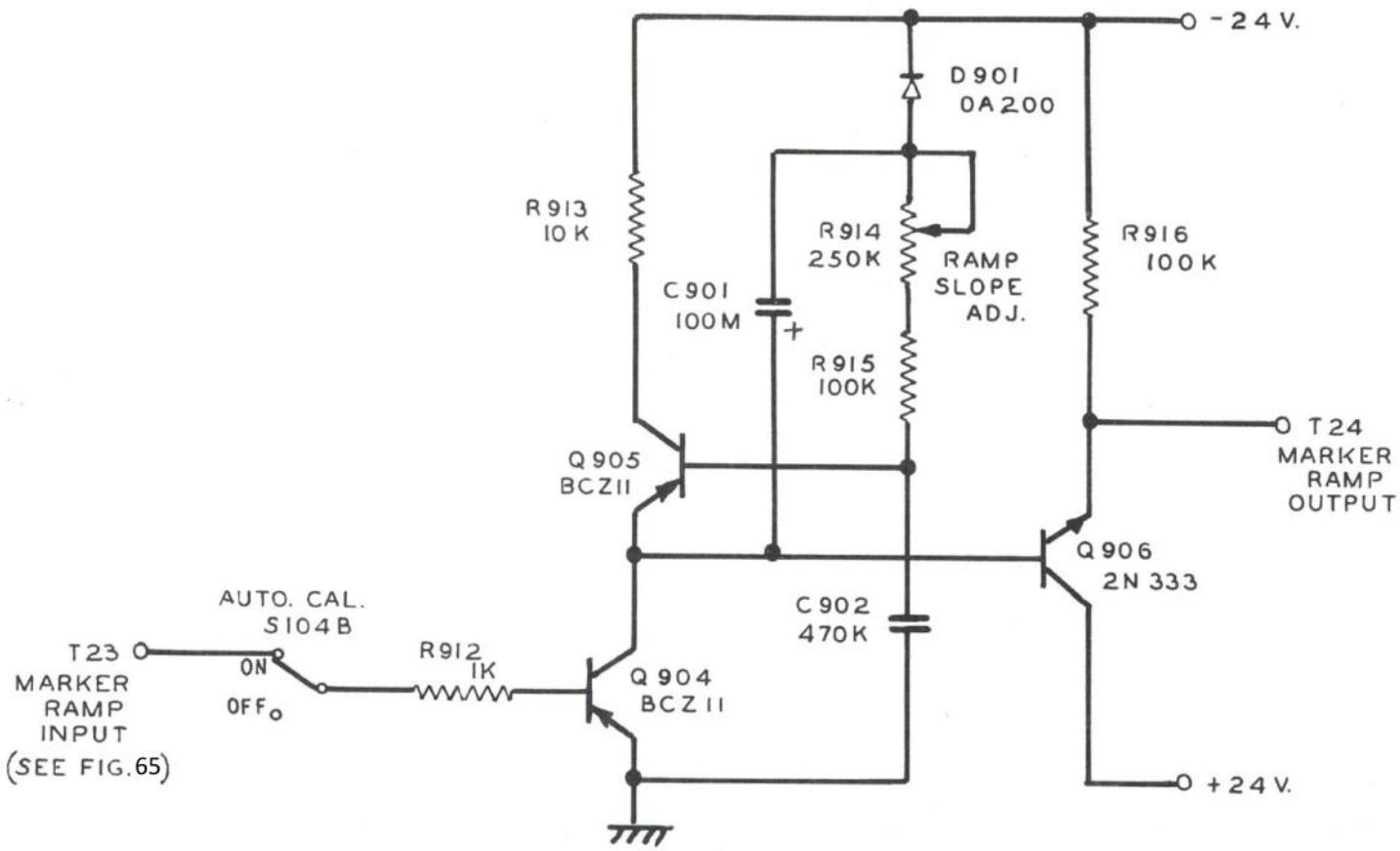


Figure 85: Marker Ramp Generator

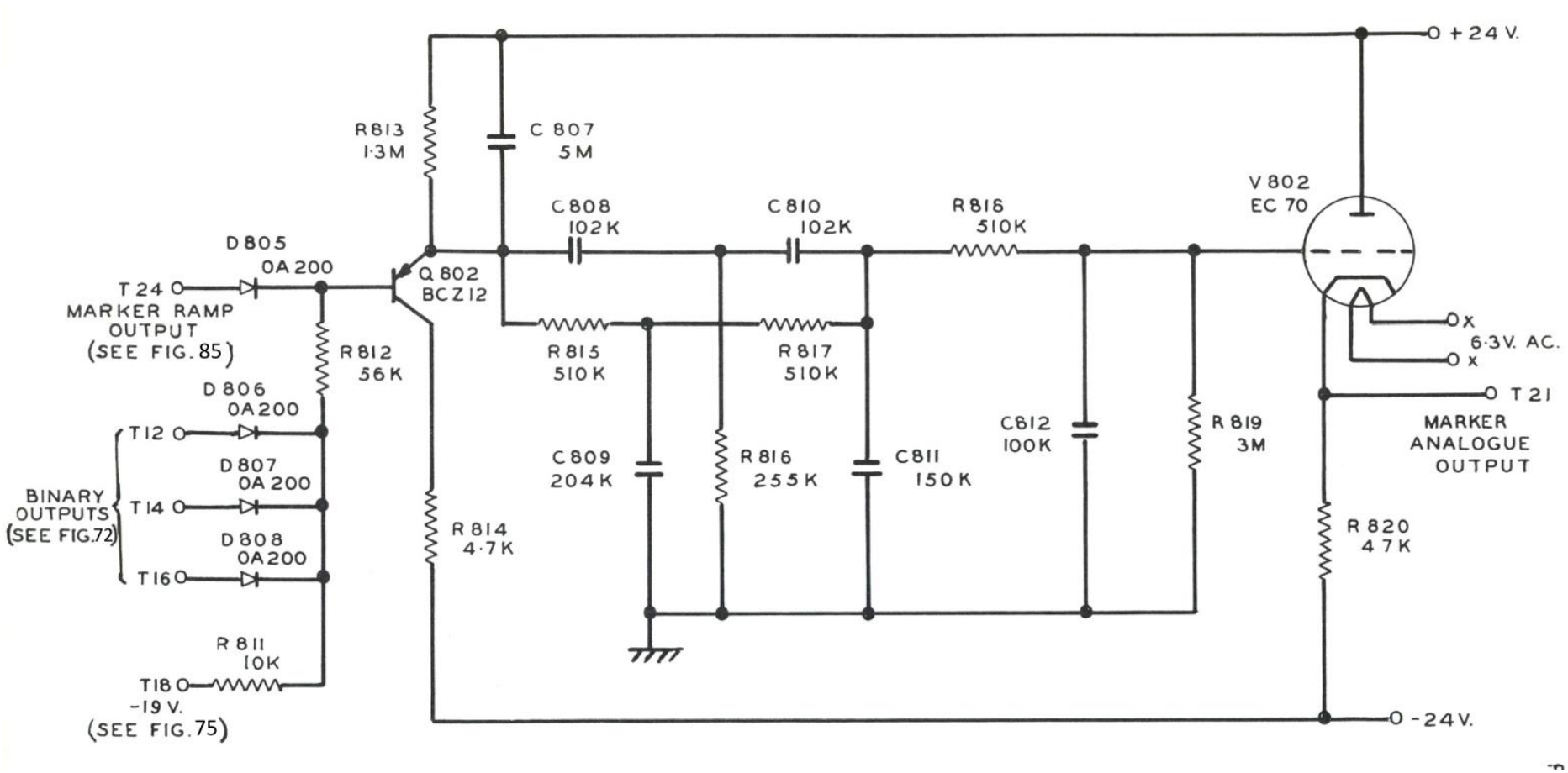


Figure 86: Marker Channel Analogue Output Voltage Generator

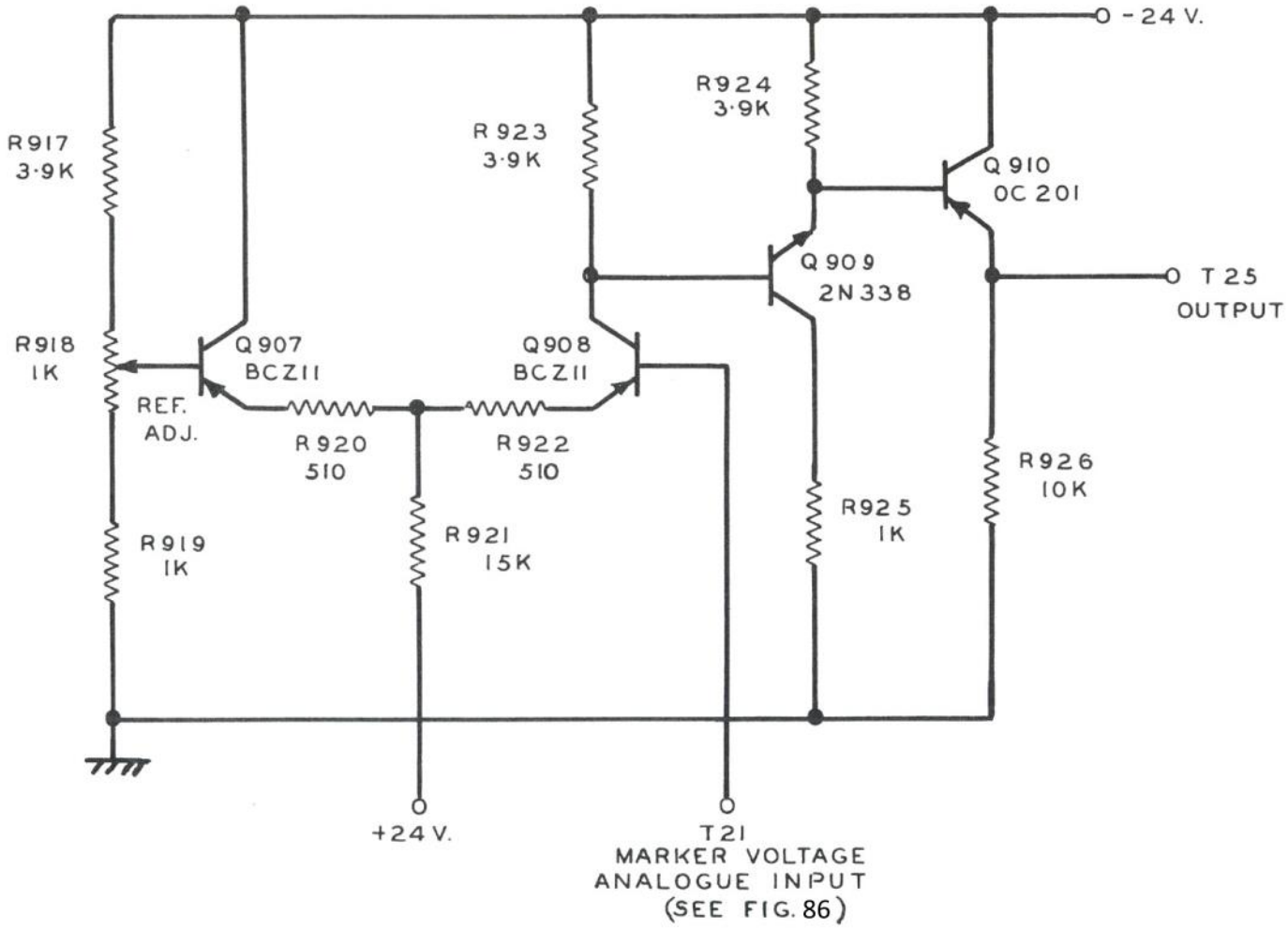


Figure 87: Marker Amplifier

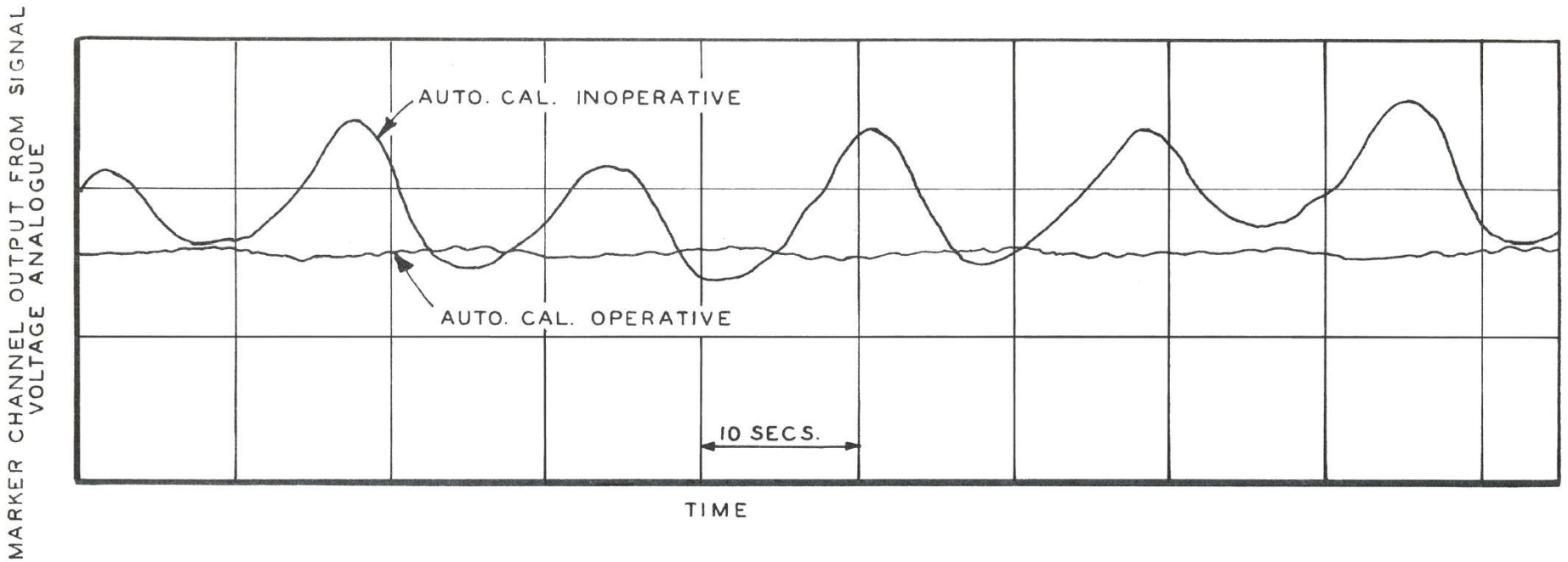


Figure 88: Graphs Illustrating the Advantage of Automatic Calibration

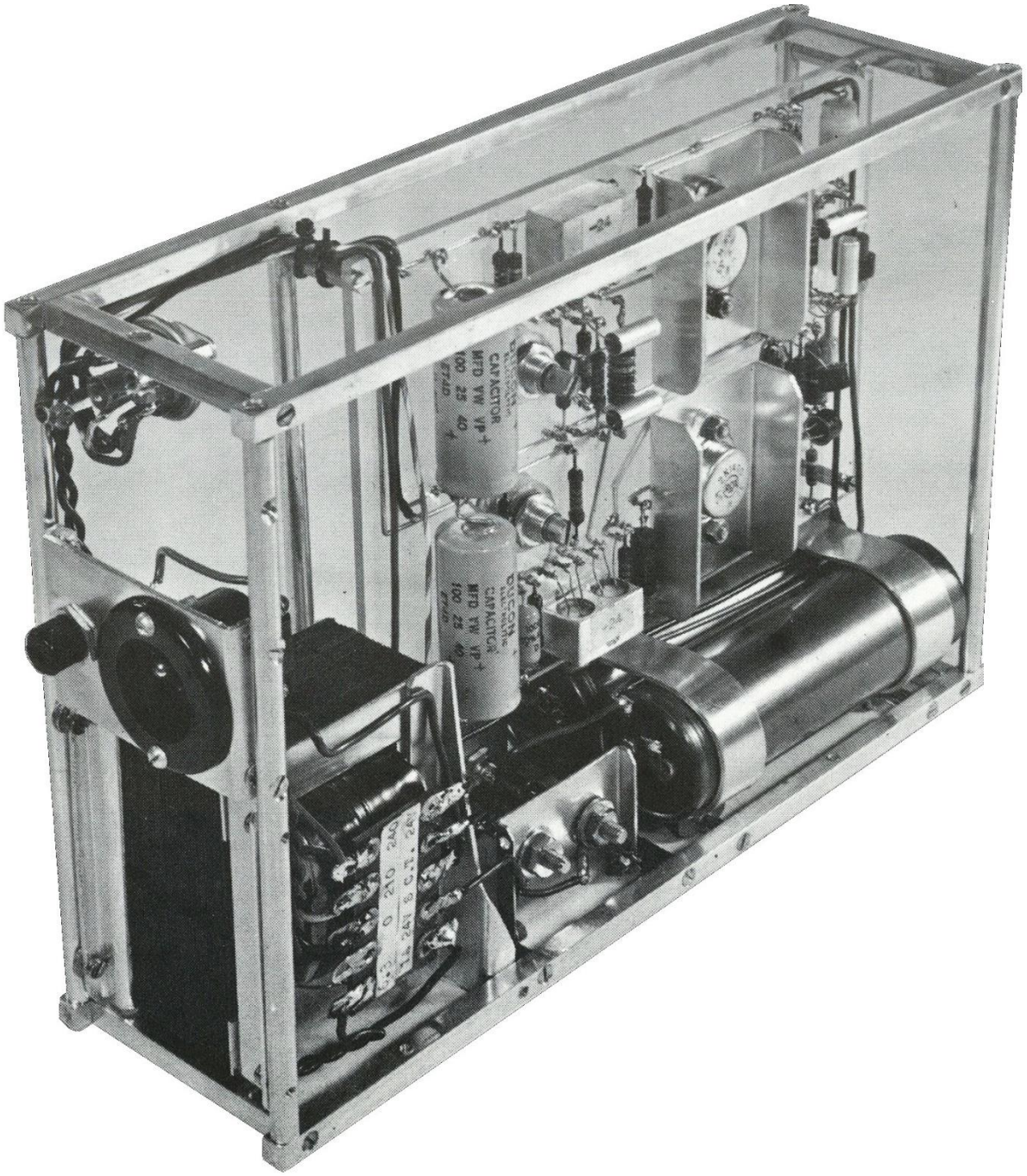


Figure 89: Ground Station Power Supply Module

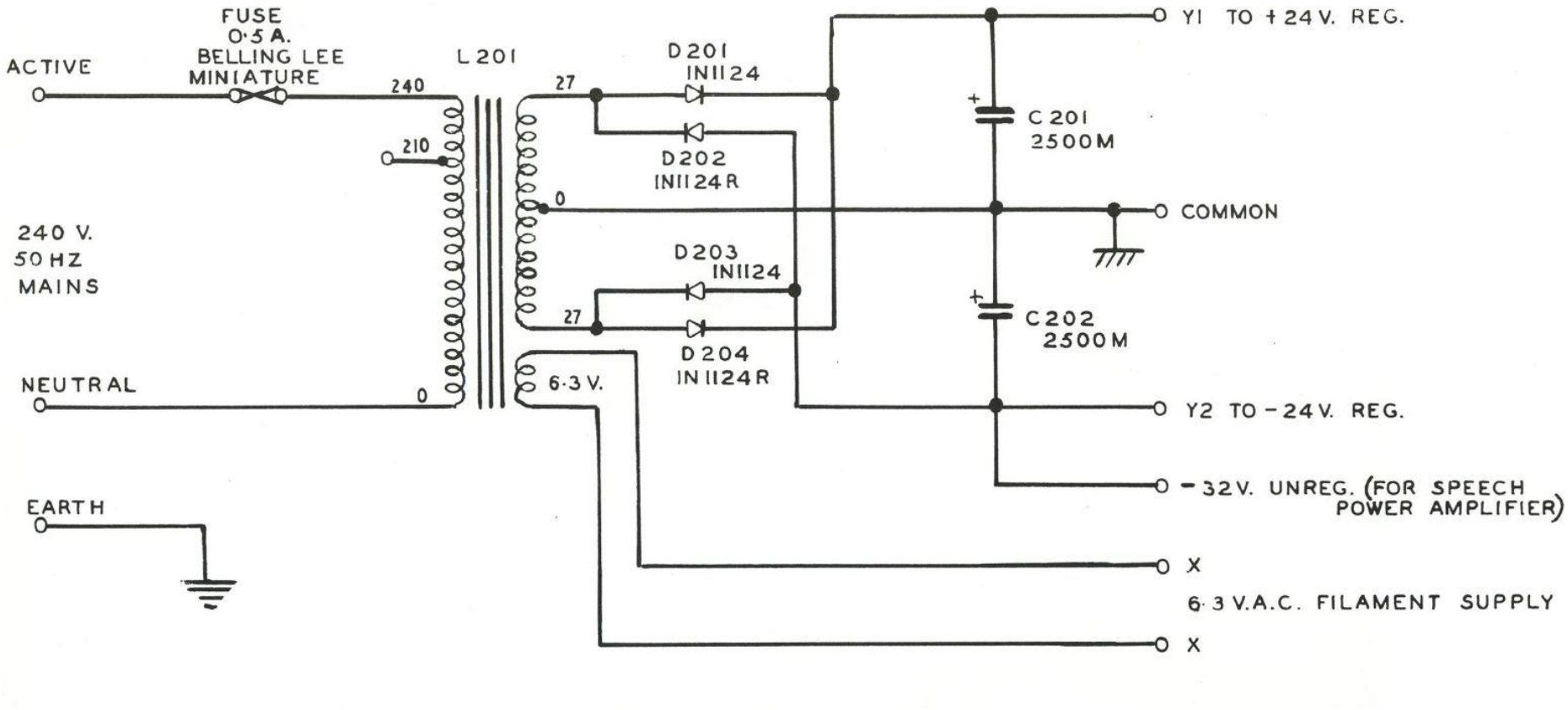


Figure 90: Transformer, Rectifier and Filter Circuit

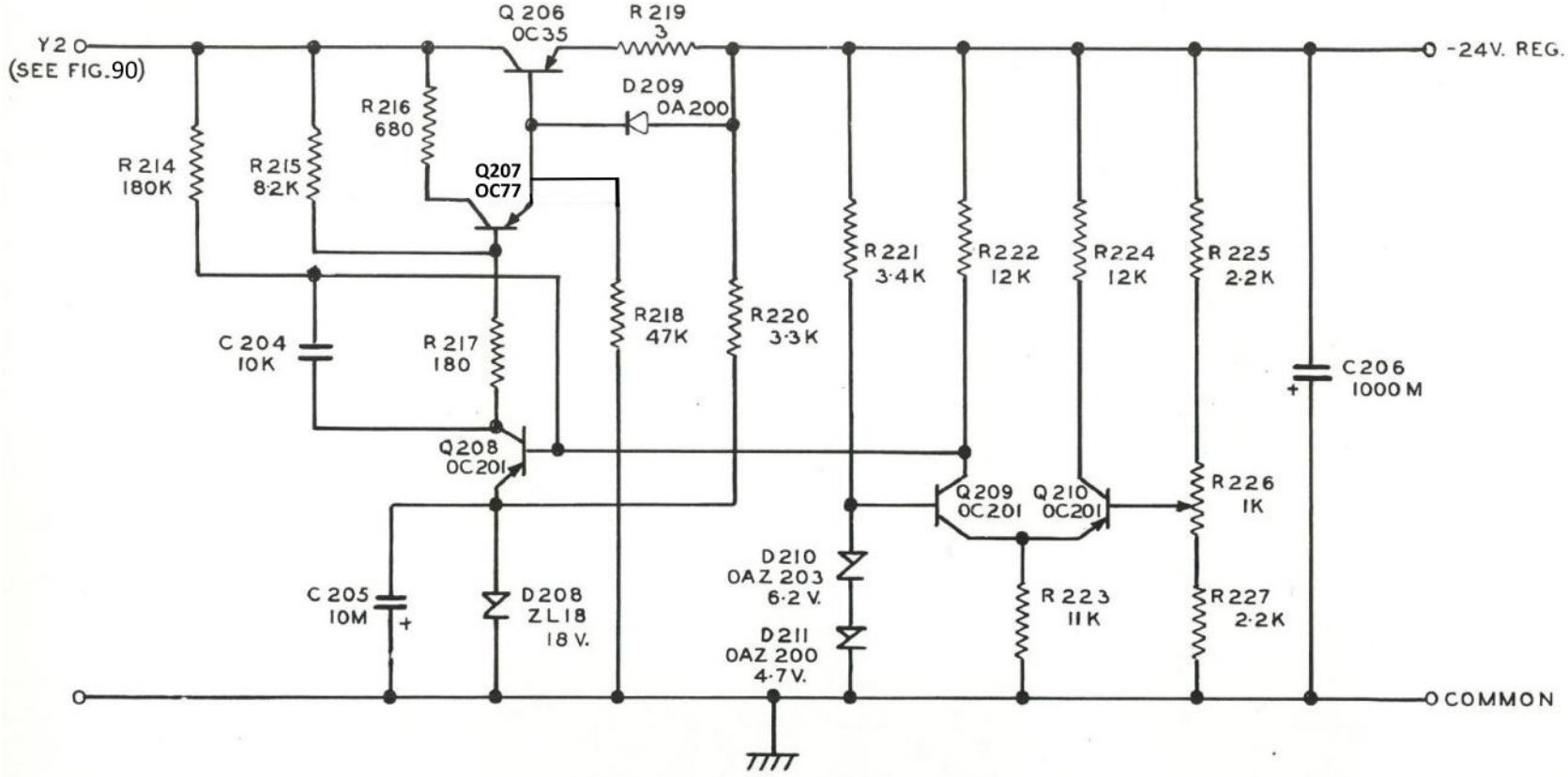


Figure 91: –24V Regulator

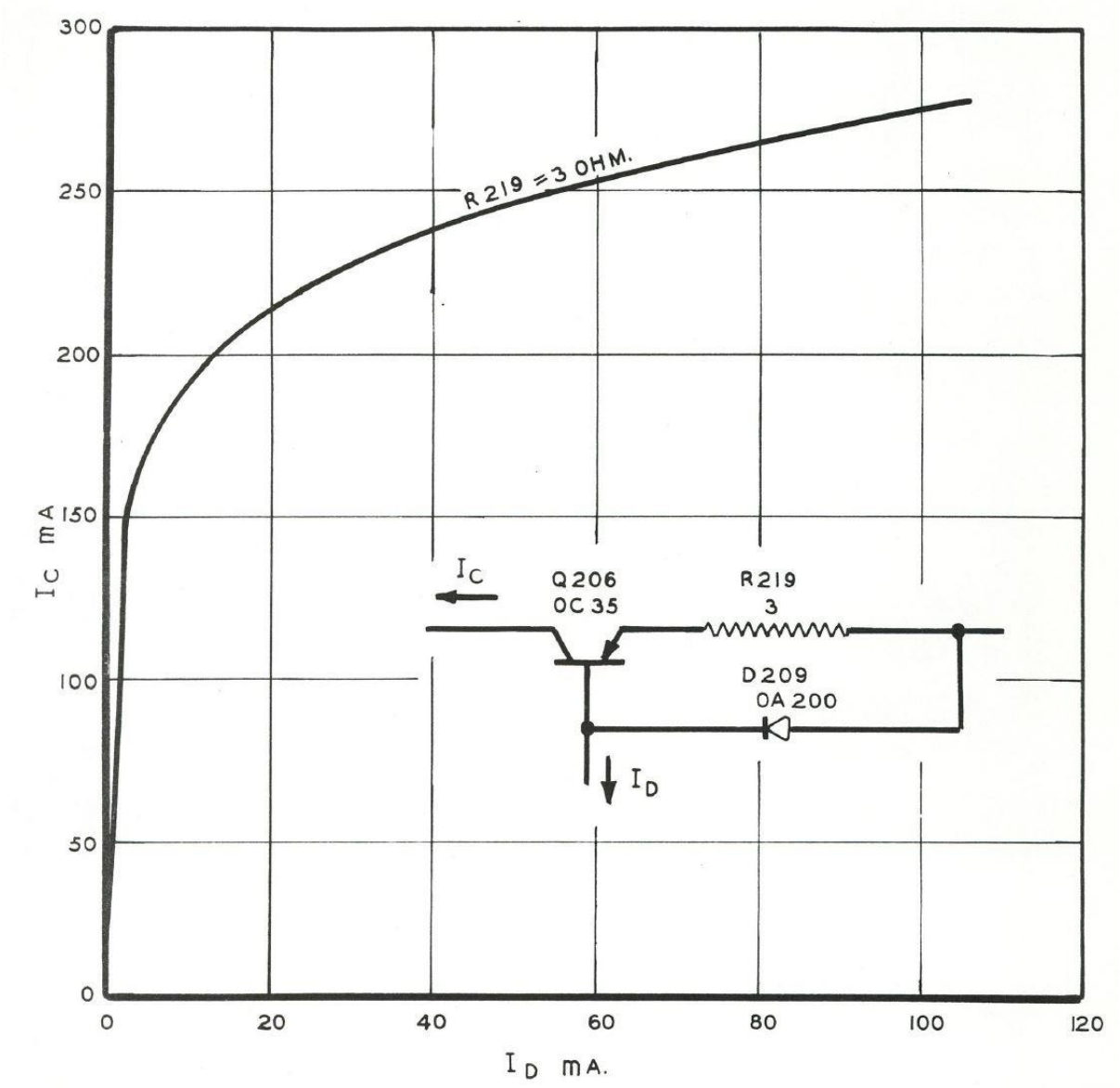


Figure 92: Current Limiting in –24V Regulator

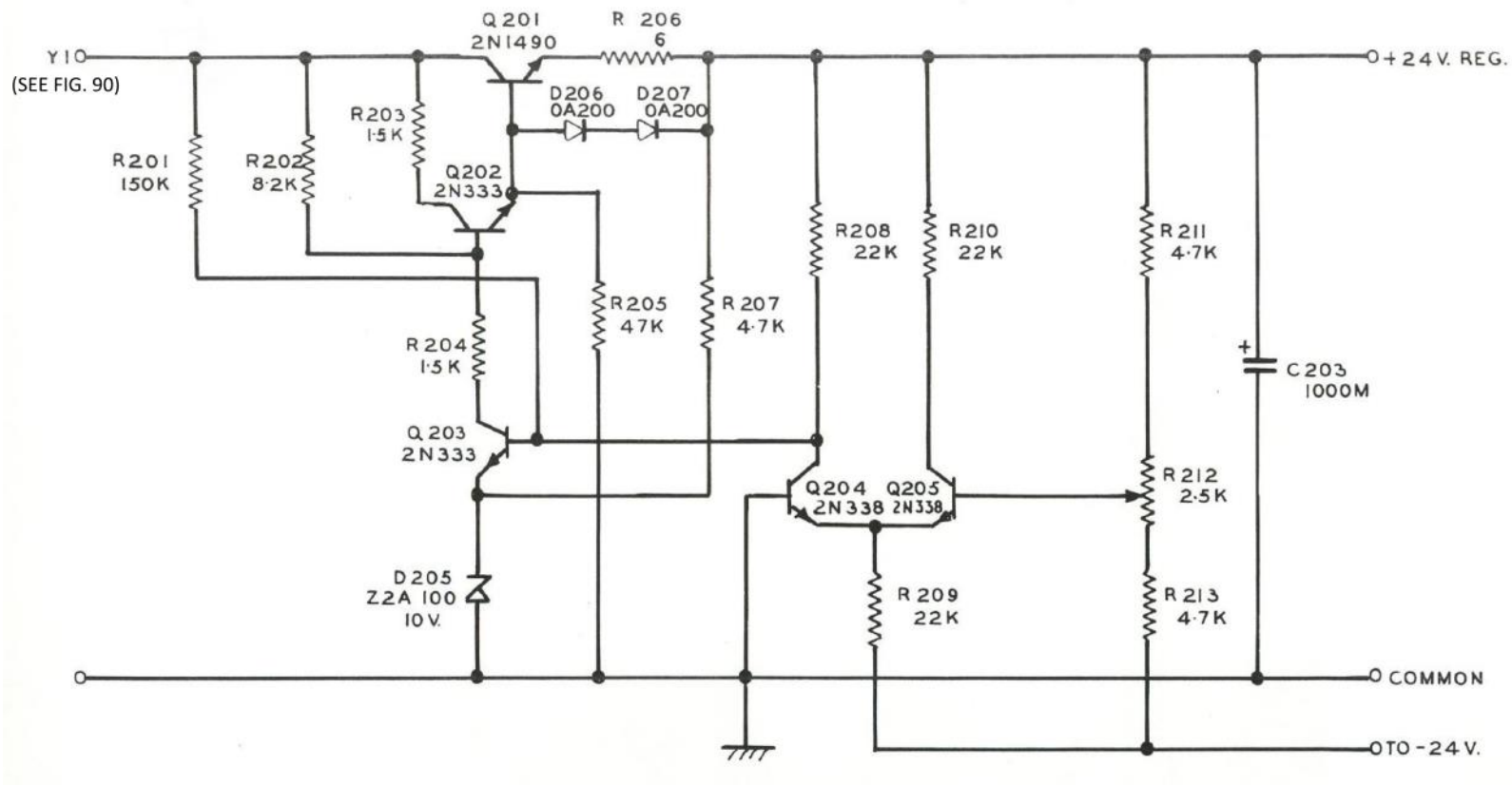


Figure 93: +24V Regulator

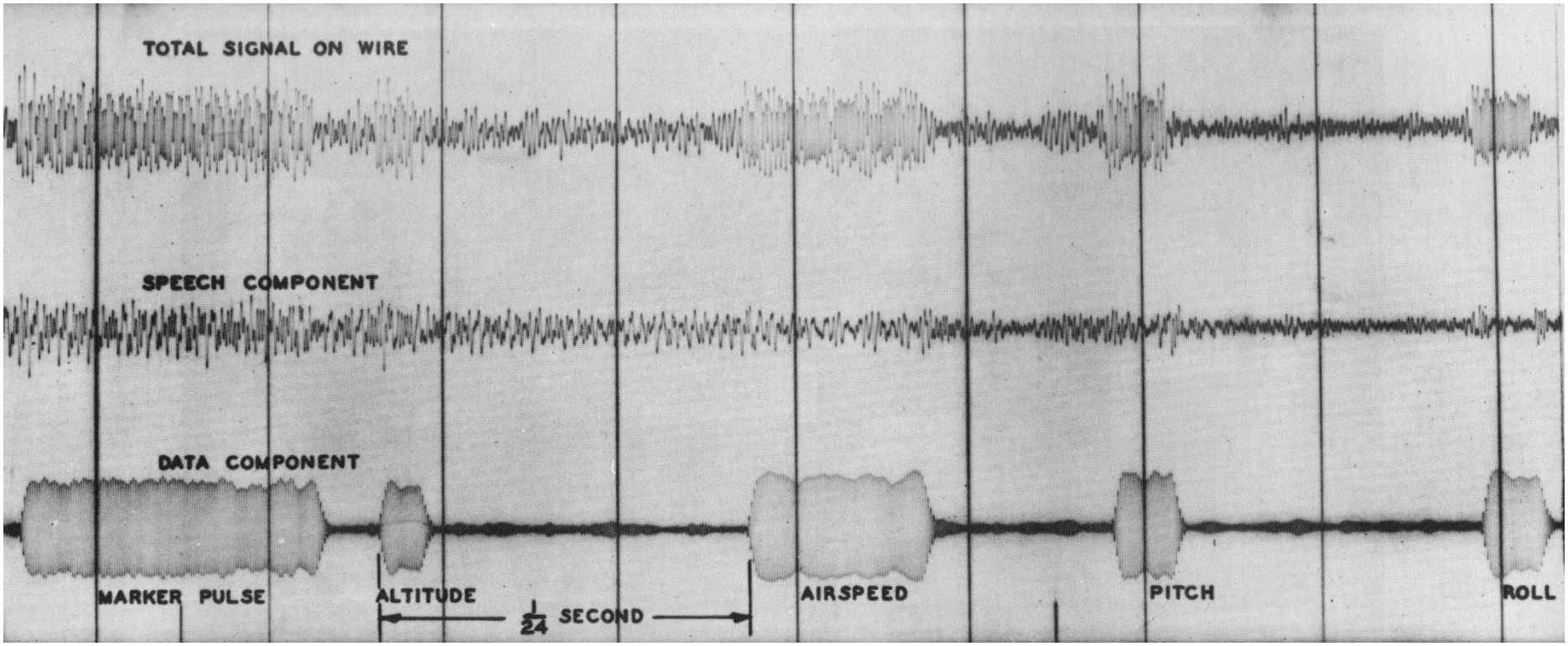


Figure 94: Oscillograms of Total Replayed Signal and its Separation into Cockpit Voice and Flight Data Components

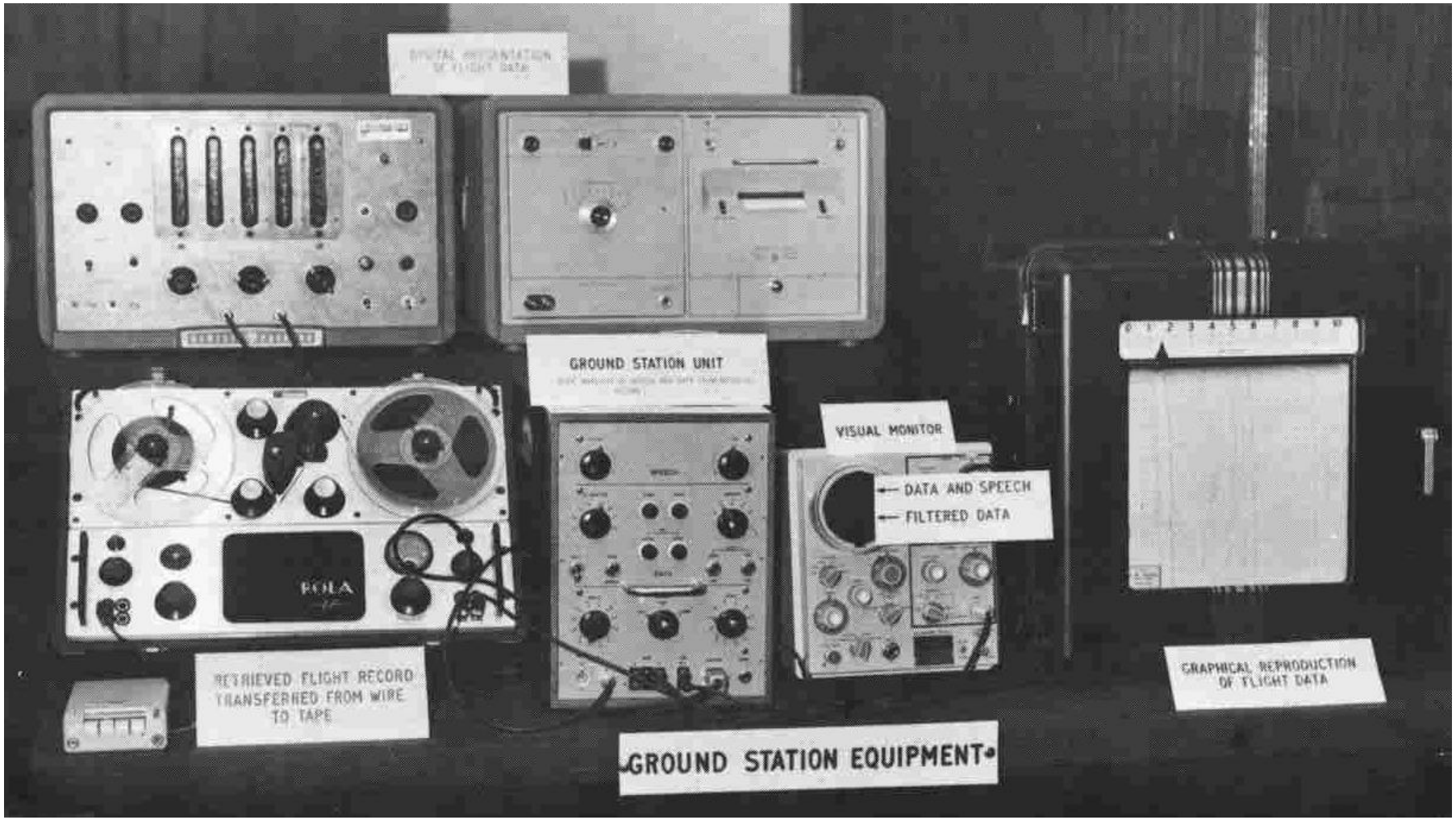


Figure 95: Photograph of Complete Ground Station

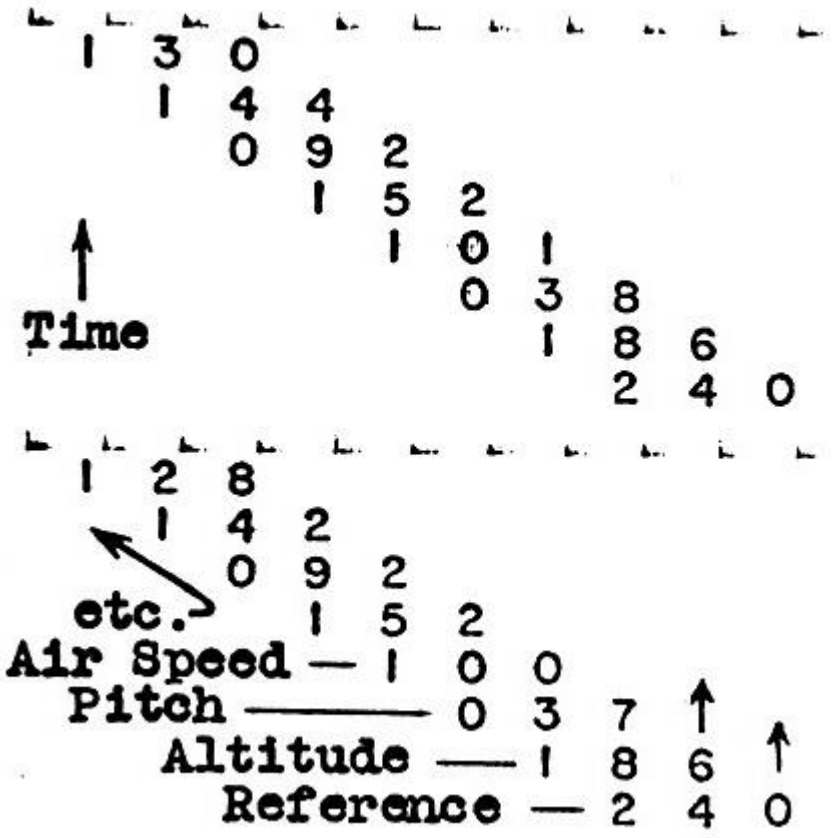


Figure 96: Electronic Counter Output of Simulated Data to Illustrate a Proposed Extension of the Single-Channel-at-a-Time Printout

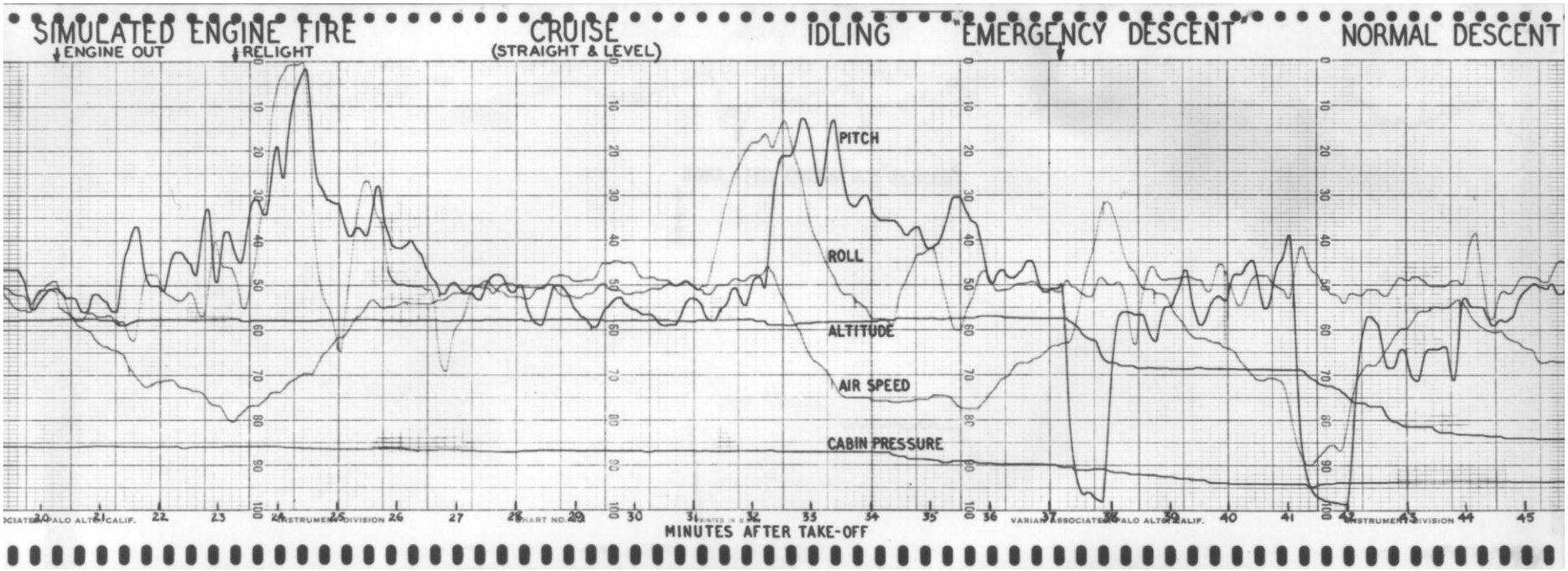


Figure 97: Original Plot of Analogue Flight Data for the 23-March-1962 Full Flight

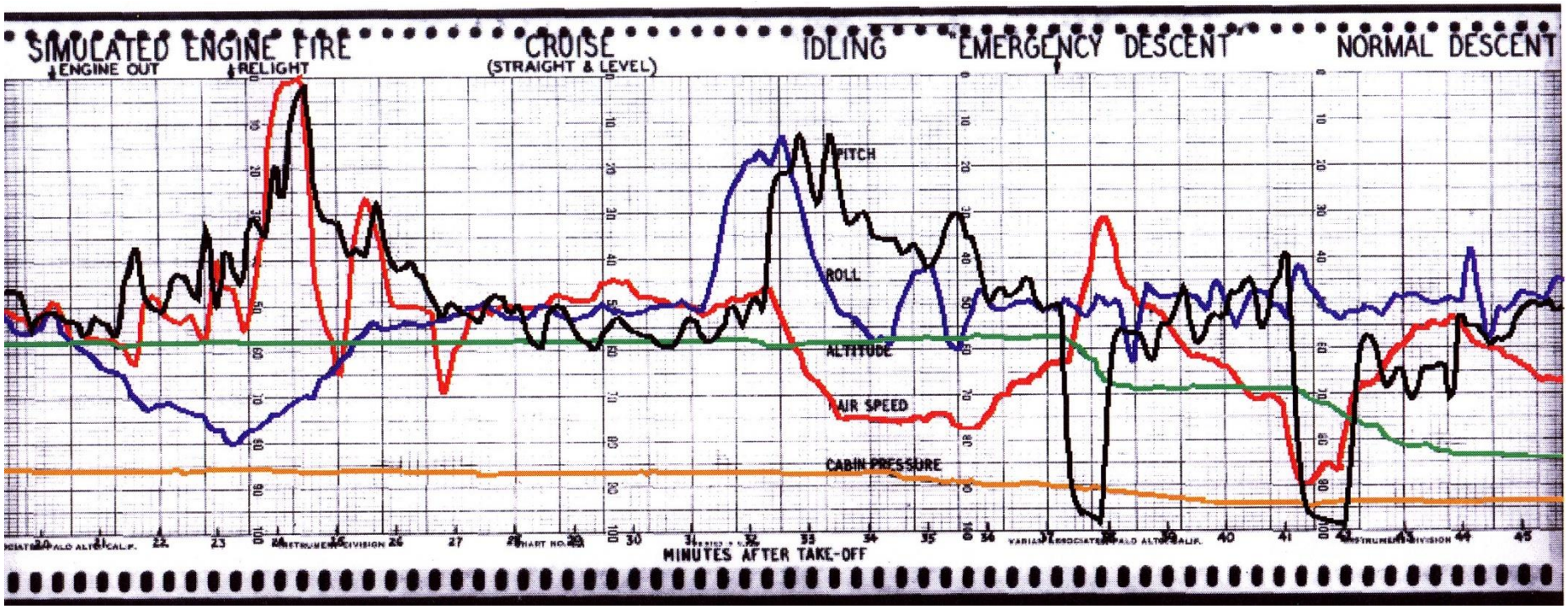


Figure 98: Colour Copy of the Analogue Flight Data for the 23-March-1962 Full Flight

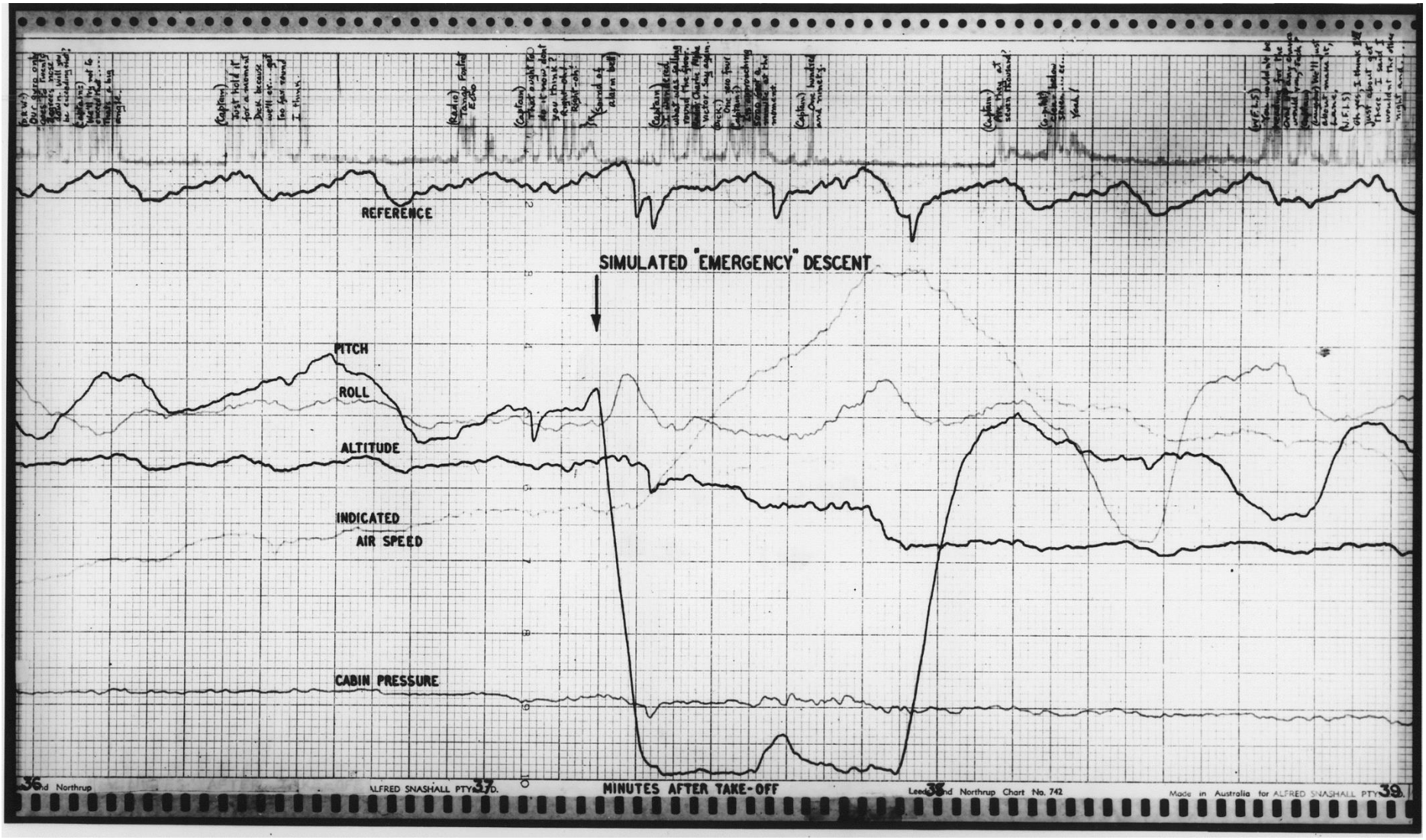


Figure 99: Original Three-Minute Analogue Voice Plus Flight Data Plot of Simulated Emergency Descent

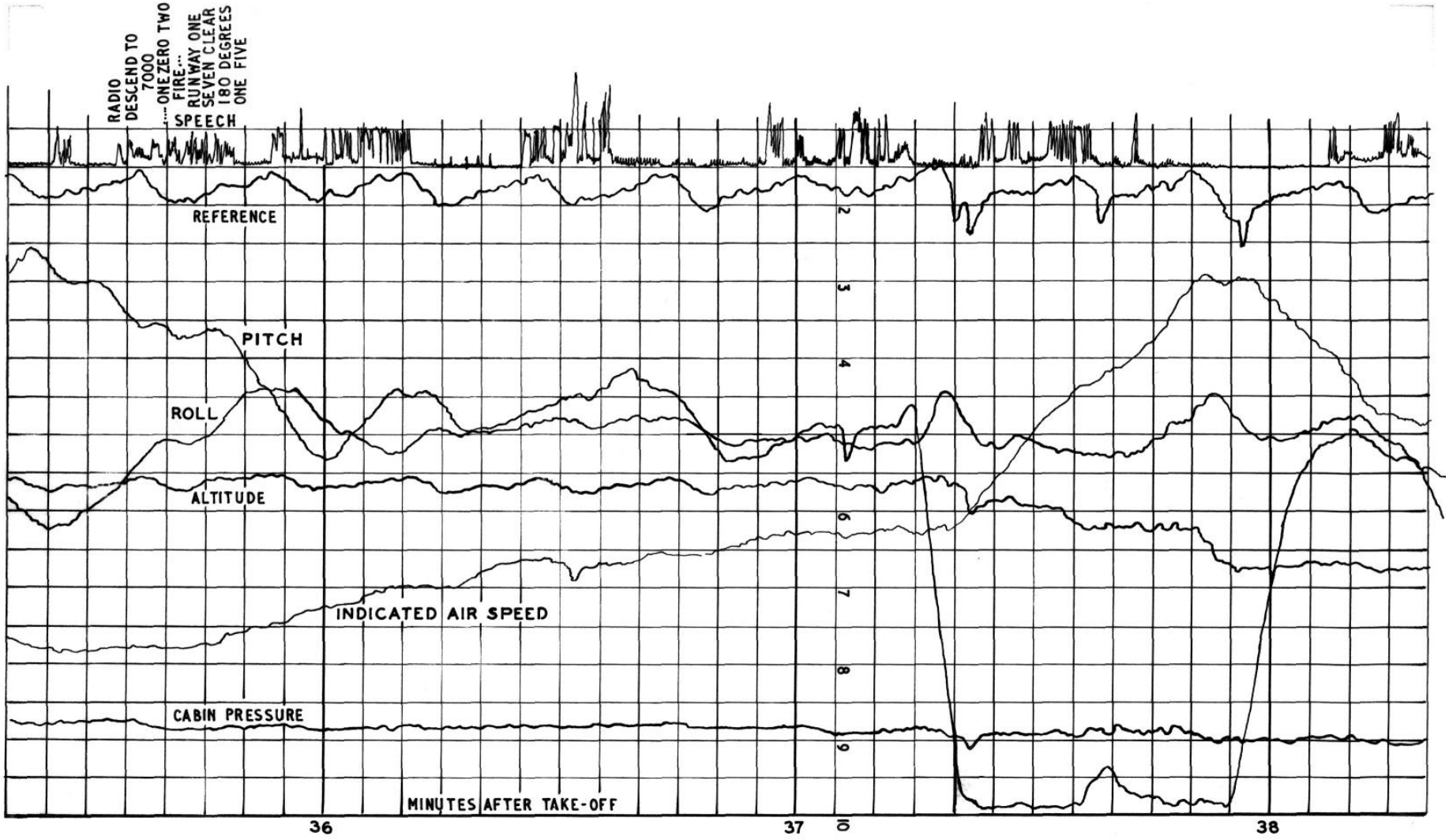


Figure 100: Redrawn Near Copy of Three-Minute Analogue Voice-Plus-Flight-Data Plot of Simulated Emergency Descent

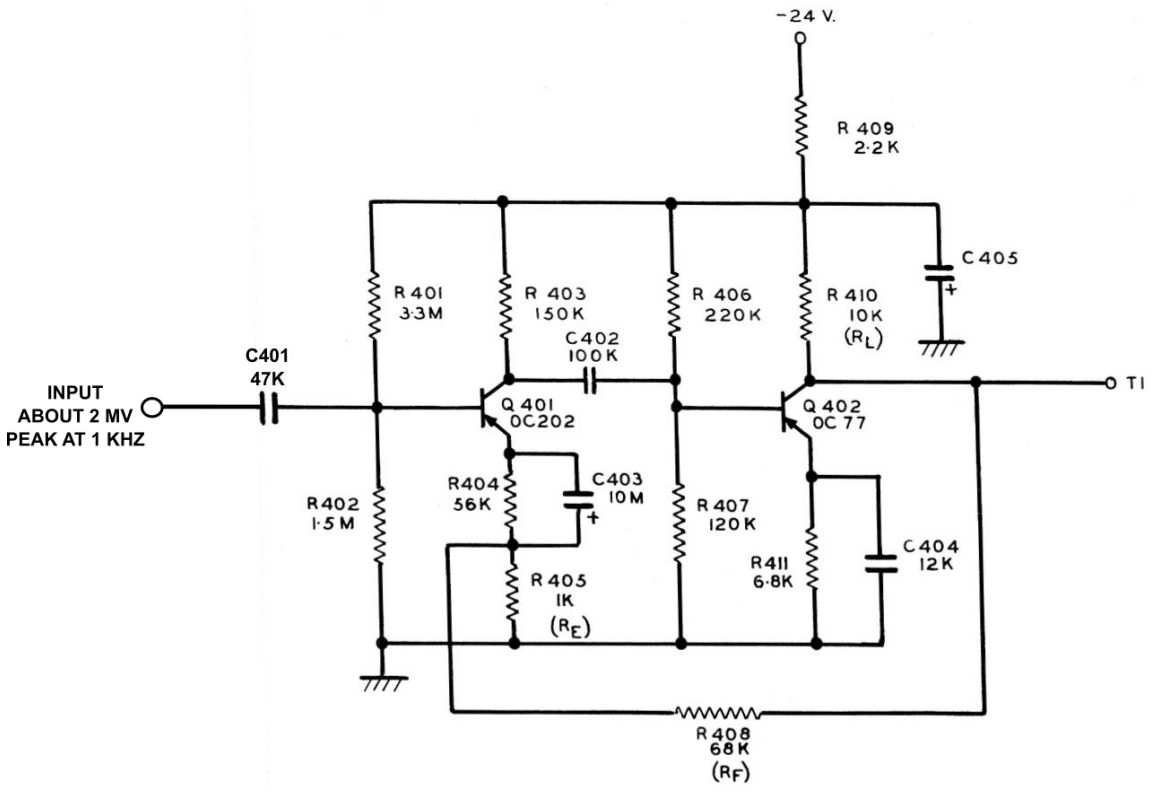


Figure A1: Flight Memory Ground Station Unit Pre-Amplifier

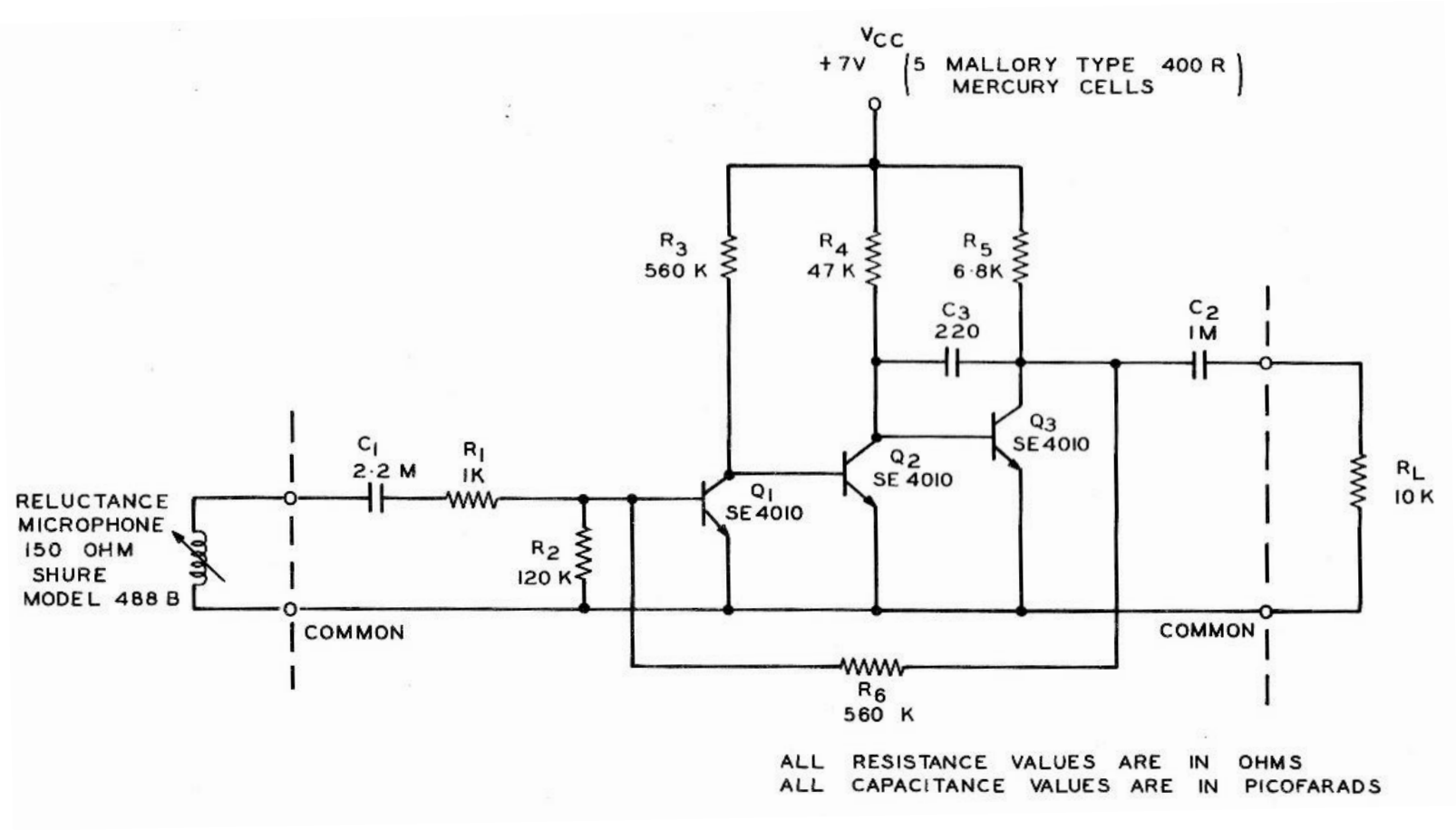


Figure A2: Sample Microphone Pre-Amplifier Circuit

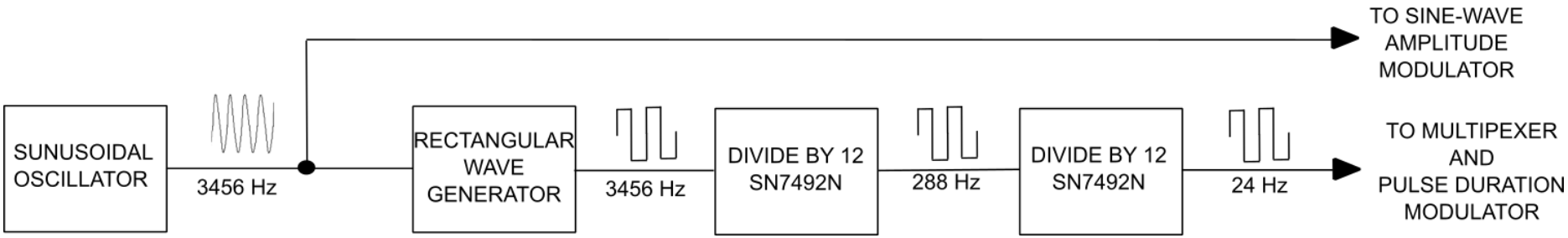


Figure A3: Alternative for Flight Data Sampling Rate Clock and Sine-wave Amplitude Modulator Carrier Frequency Generation

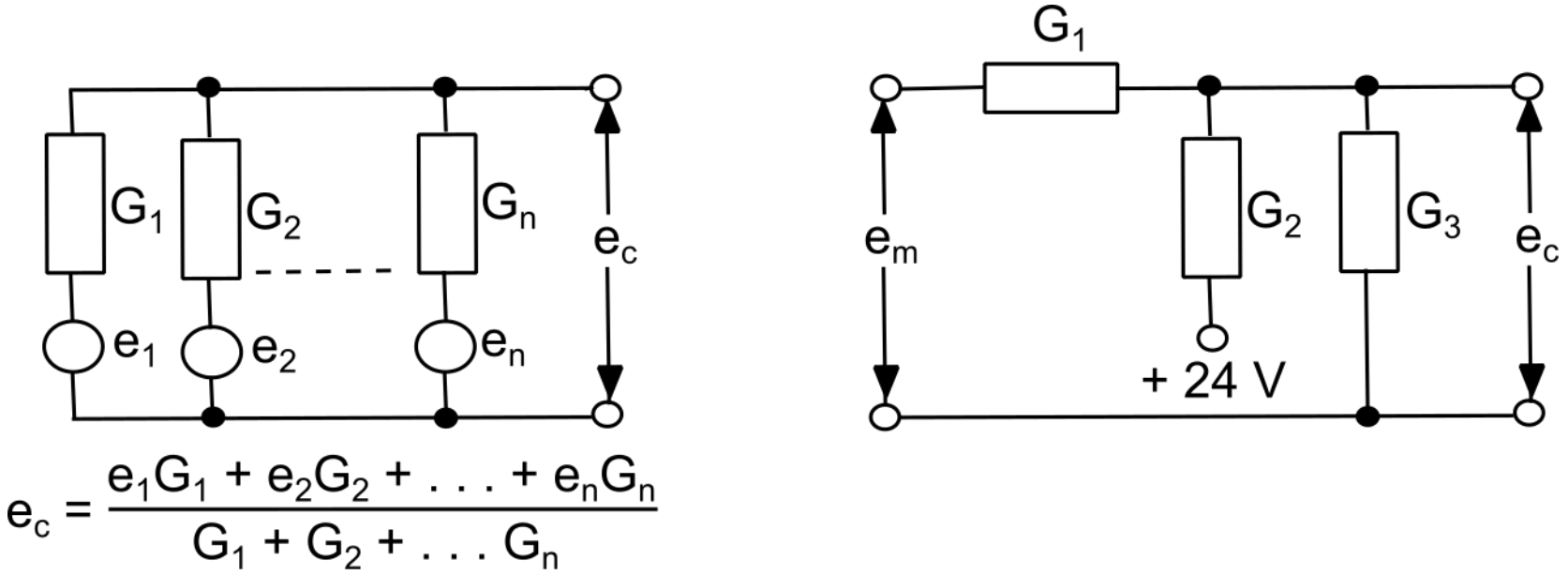


Figure A4: Analog Output Offset Producer

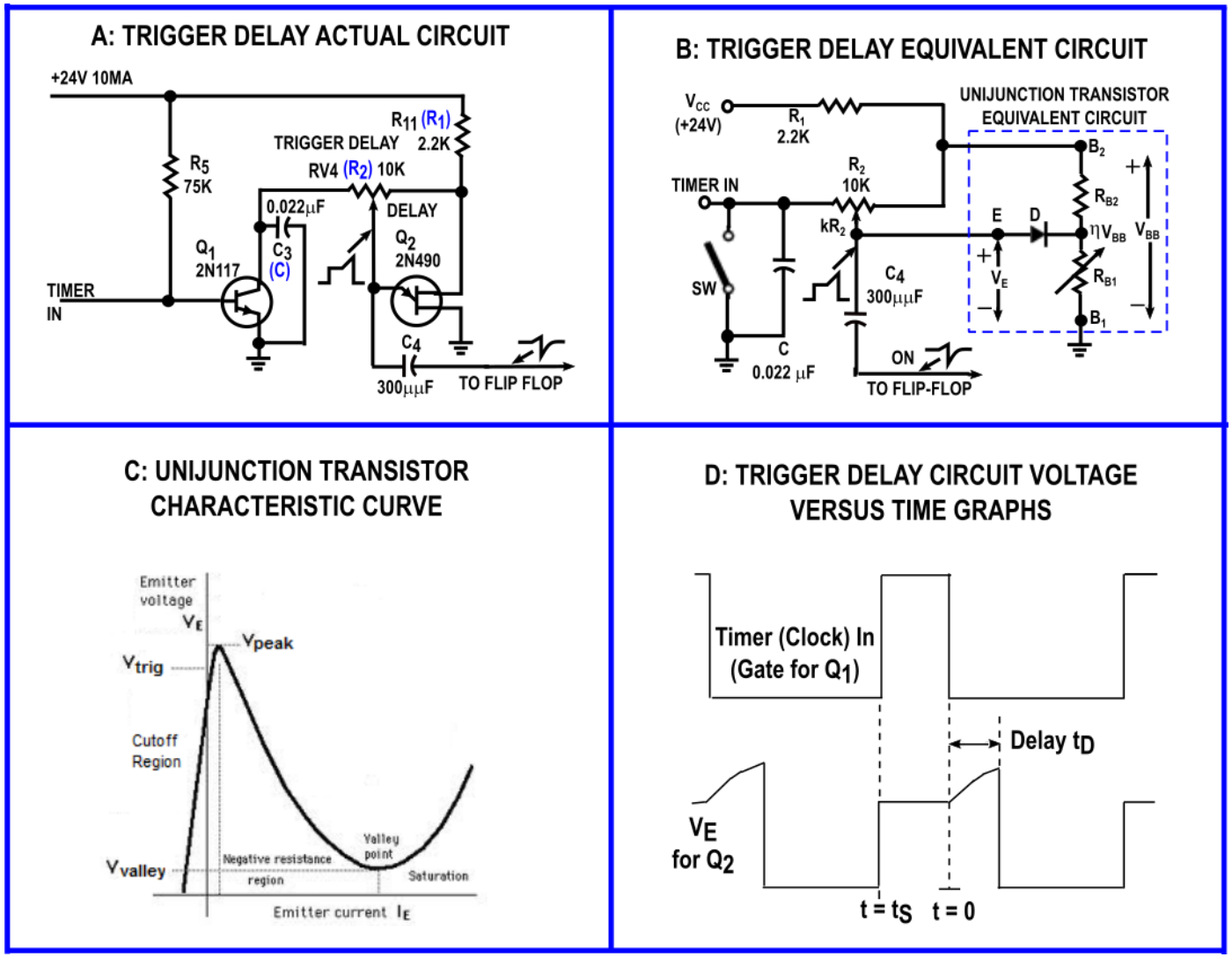


Figure A5: Pulse Duration Modulator Trigger Delay Circuits and Graphs

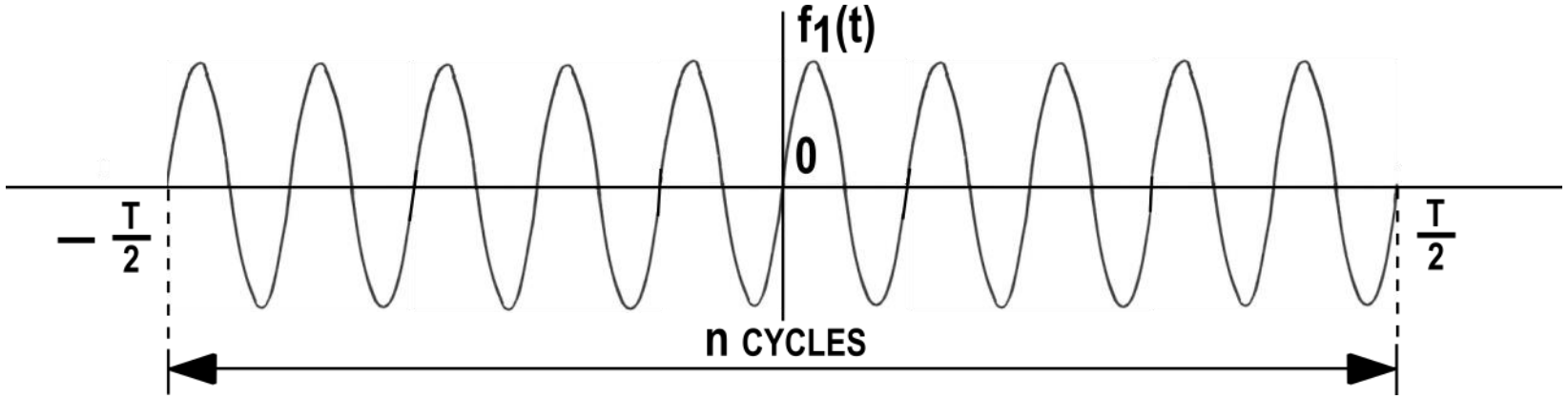


Figure A6: Sine-Wave Burst Defined by: $f_1(t) = \sin(2\pi f_0 t)$ in range $\left(-\frac{T}{2} < t < \frac{T}{2}\right)$ for $n = 10$

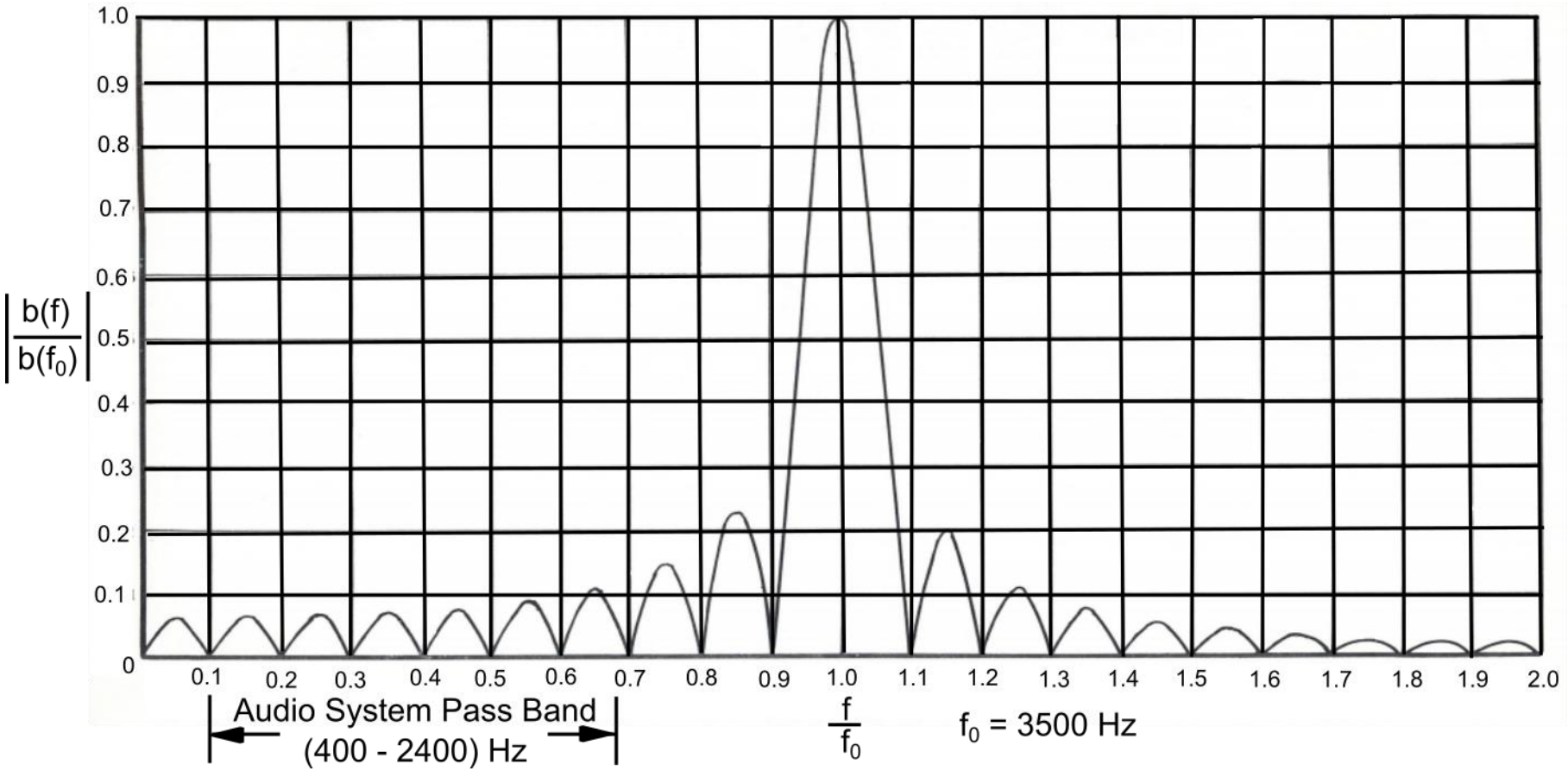


Figure A7: Frequency Spectrum of a 10-Cycle Burst of 3500 Hz Sine Waves

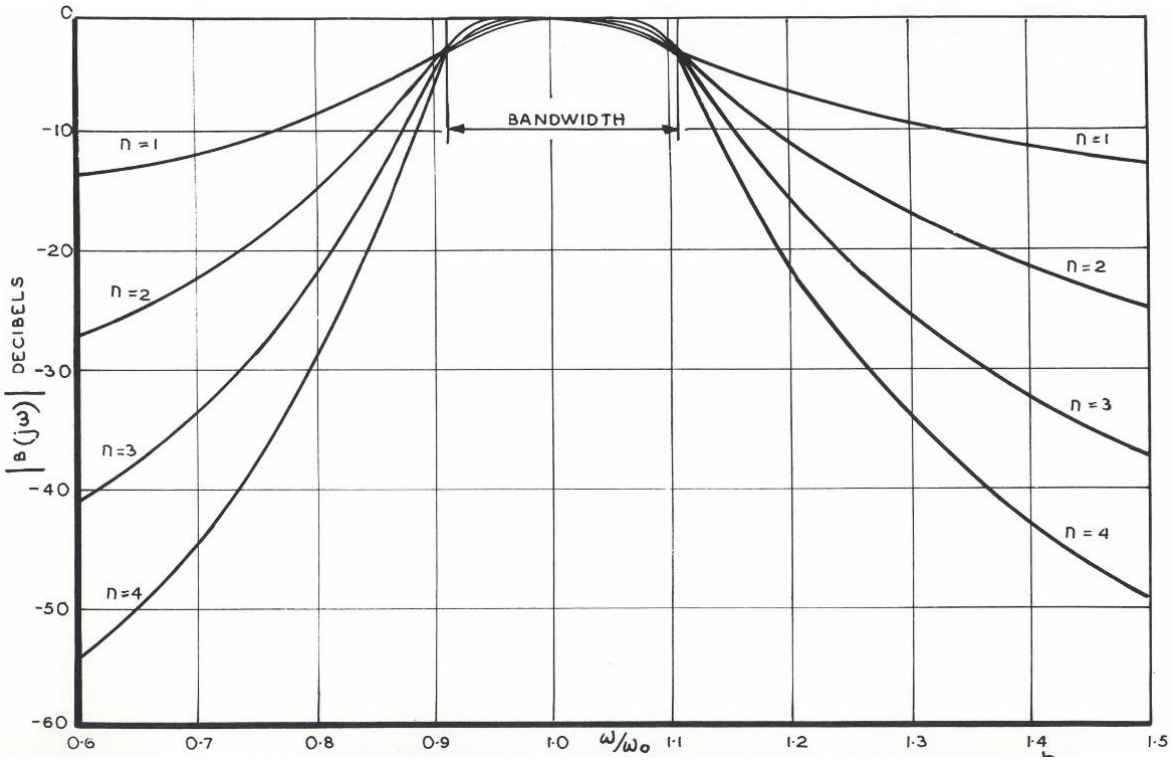


Figure A8: Frequency Responses of Maximally Flat Band-Pass Filters

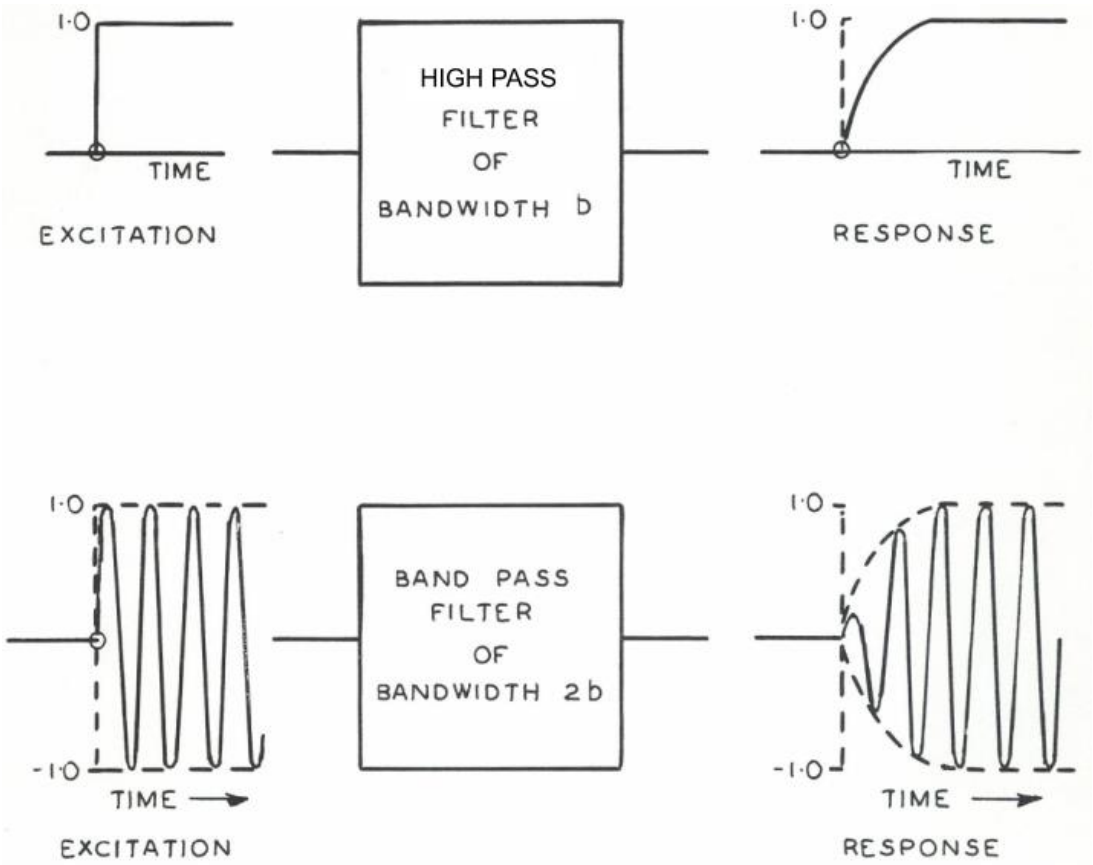


Figure A9: Amplitude Response of Band-pass Filter in Terms of the Equivalent High Pass Filter

N70 Fig 11

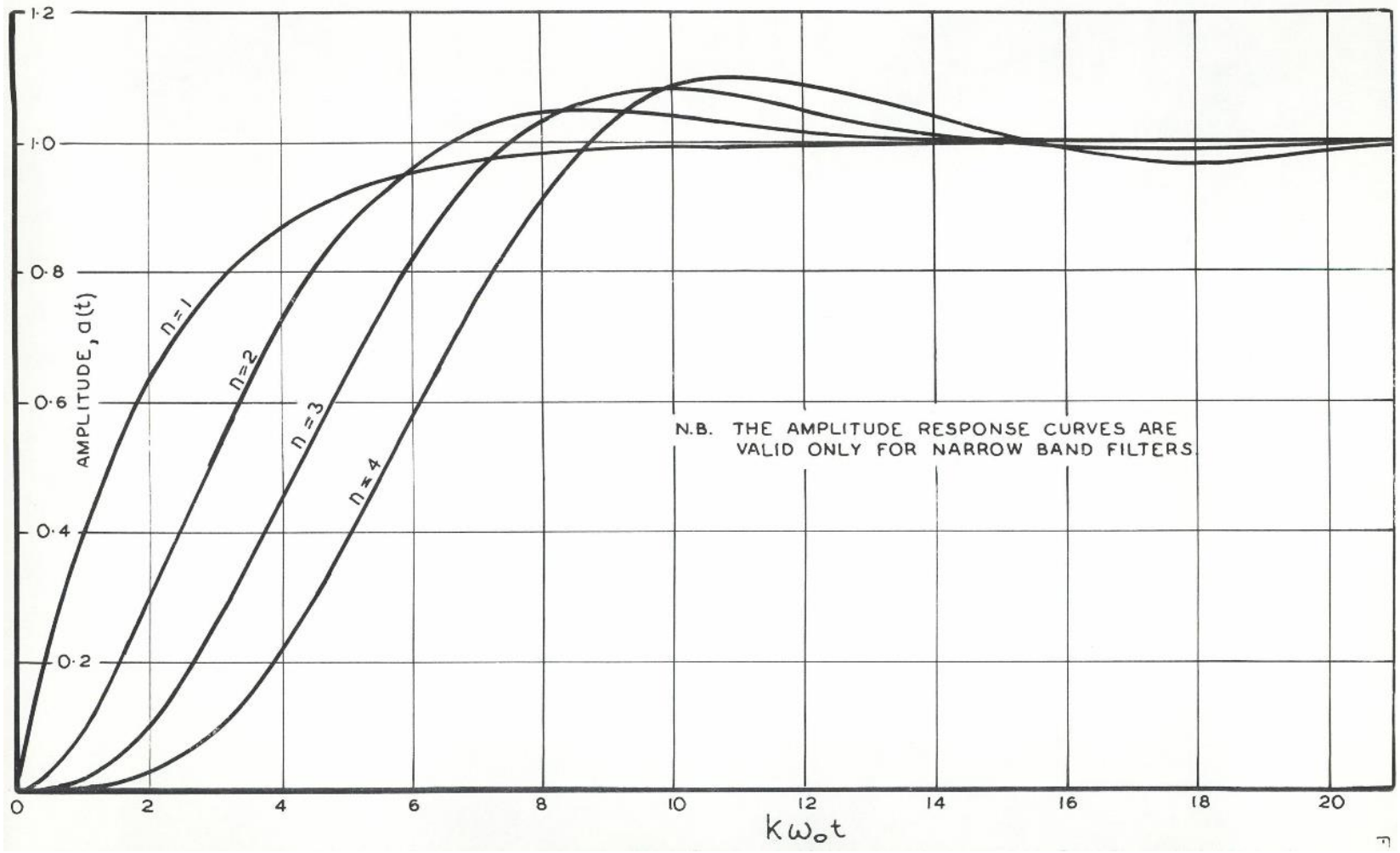


Figure A10: Amplitude Responses of Bandpass Filters Having Maximally Flat Amplitude Characteristics

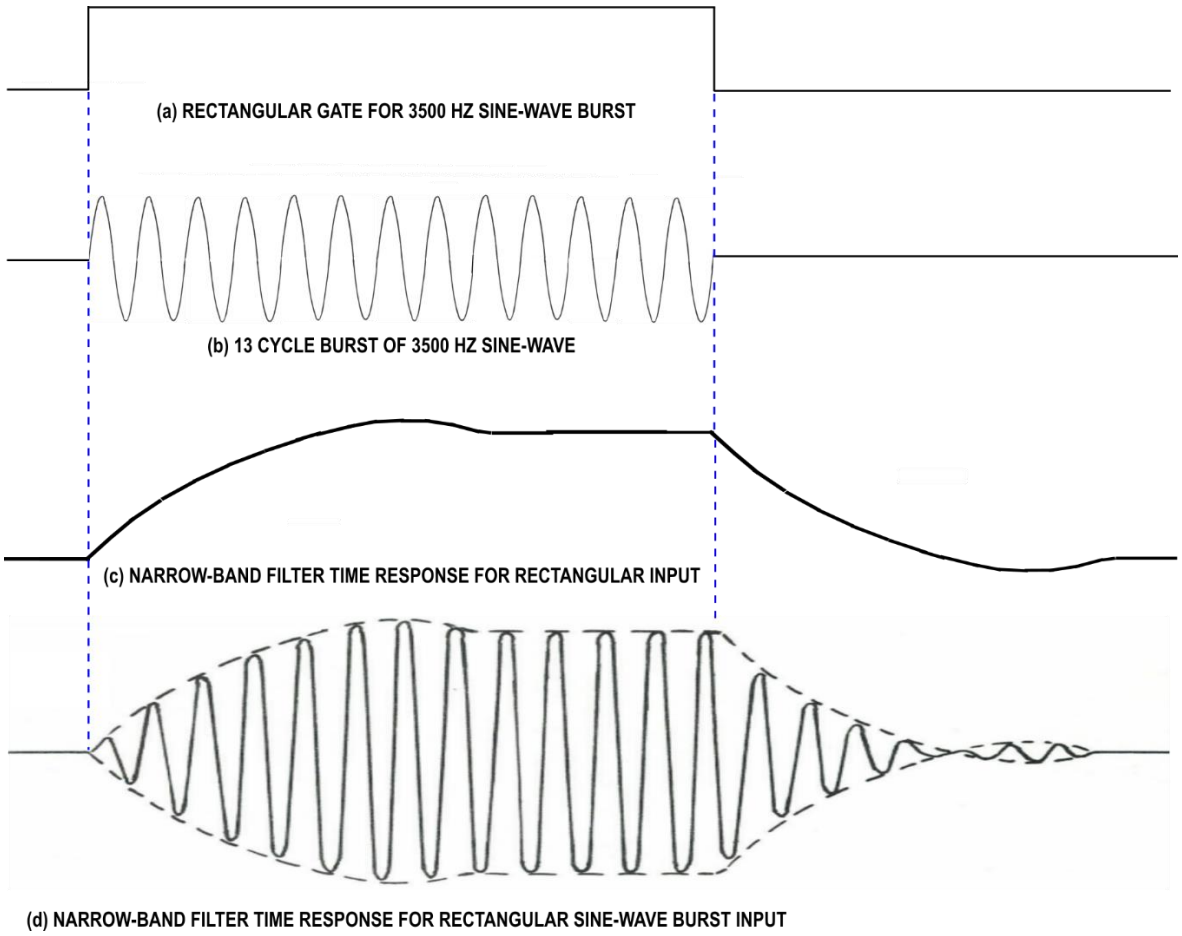


Figure A11: Comparison of a Band-Pass Filter Time Response for a Rectangular Input with that for a Sine-Wave Burst Input

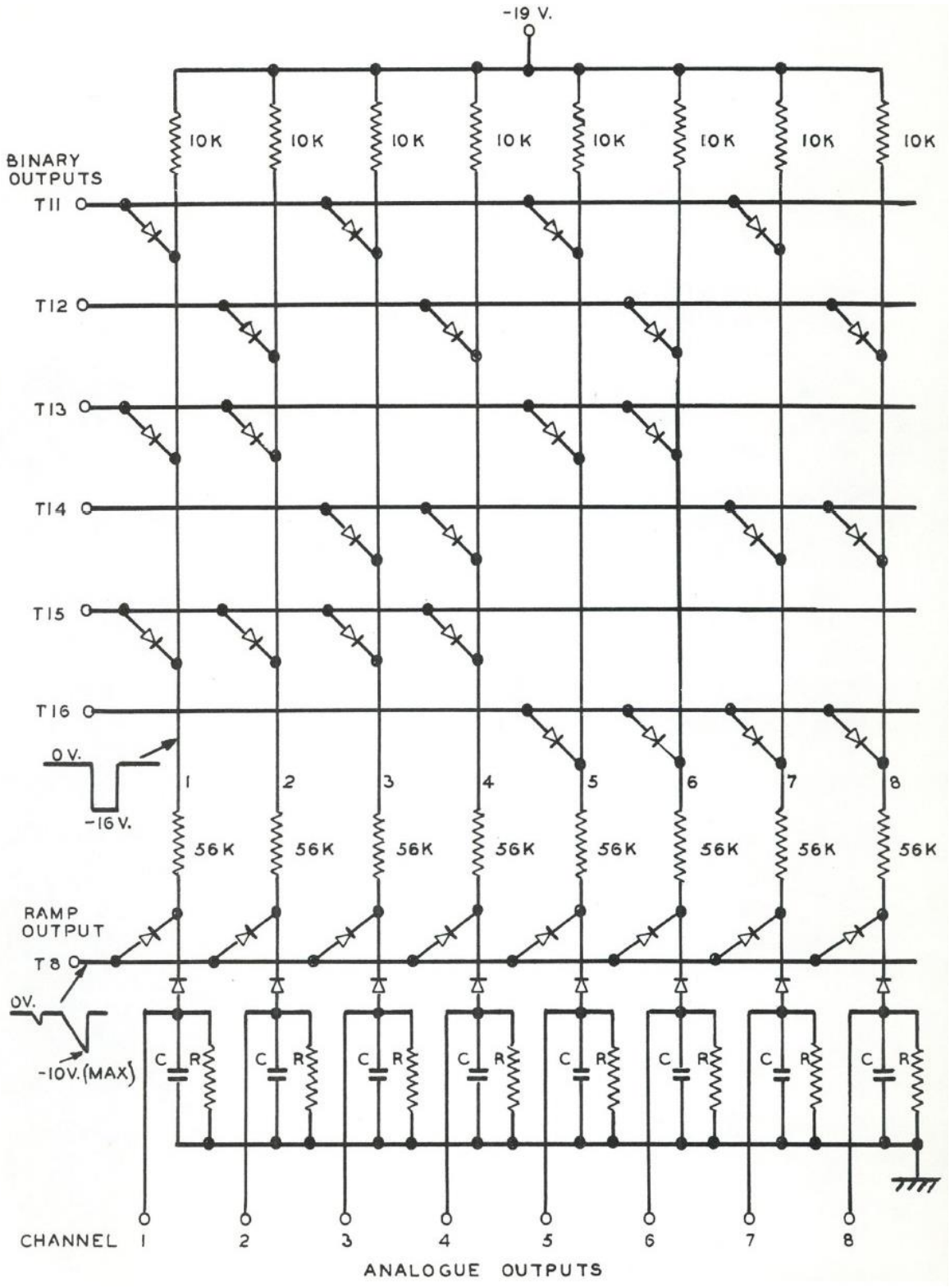


Figure A12: Simple Circuit for Simultaneous Analogue Voltage Output of All Channels